ZZZ2	ZZZ1	ZZZ3	ZZZ4	ZZZ5	ZZZ6	ZZZ7	ZZZ8
PCB DAZ@	LA-7811P DA2@	LS-6951P DA2@	LS-6953P DA2@	LS-6955P DA2@	LS-6956P DA2@	LS-6957P DA2@	LS-6958P DA2@

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QLA01 LA7811P Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point

AIO M/B

2011-06-02

REV:0.1

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.			
Title	Cover Page		
Size: Custom	Document Number: QLA01 M/B LA-7811P Schematic		Rev: 1.A
Date: Thursday, June 09, 2011	Sheet 1 of 63		

Compal Confidential

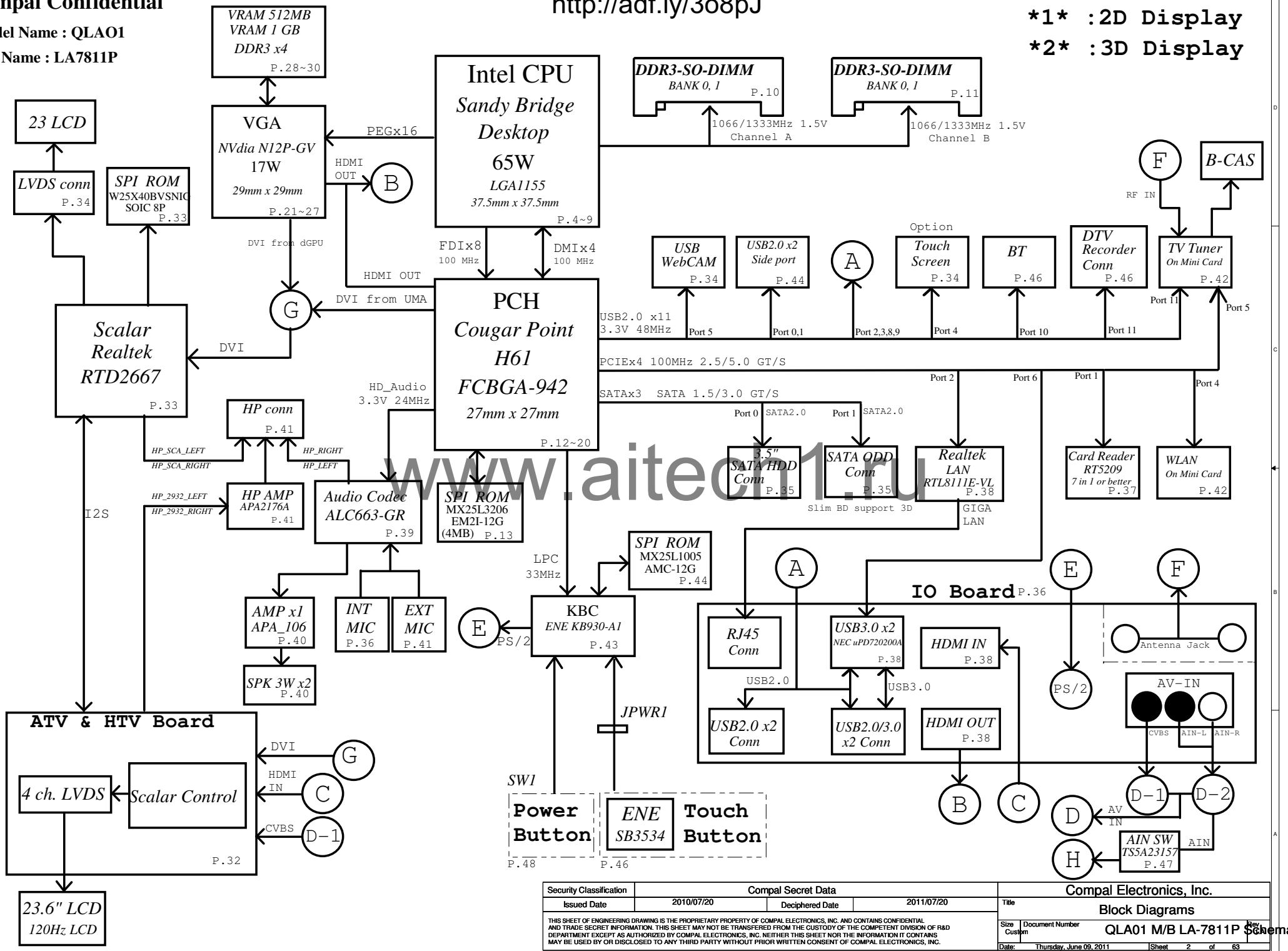
Model Name : QLAO1

File Name : LA7811P

http://adf.ly/3o8pJ

***1* :2D Display**

***2* :3D Display**



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: Block Diagrams

Size: Custom | Document Number: QLA01 M/B LA-7811P | Rev: Schematic

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DMI_PTX_HRX_N[0..3] 14
DMI_PTX_HRX_P[0..3] 14
DMI_HTX_PRX_N[0..3] 14
DMI_HTX_PRX_P[0..3] 14

PEG_GTX_C_HRX_P[0..15] 22
PEG_GTX_C_HRX_N[0..15] 22
PEG_HTX_C_GRX_P[0..15] 22
PEG_HTX_C_GRX_N[0..15] 22

JCPU1C SKT_H2

<REV>

Note:Use 0.1uF now; If need to support to Gen3, need change C1~C32 to 0.22uF.

PEG_GTX_C_HRX_P15	B11	PEG_RX[0]	PEG_TX[0]	C13	PEG_HTX_GRX_P15	C1	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_P15
PEG_GTX_C_HRX_N15	B12	PEG_RX#[0]	PEG_TX#[0]	C14	PEG_HTX_GRX_N15	C2	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_N15
PEG_GTX_C_HRX_P14	D12	PEG_RX[1]	PEG_TX[1]	E14	PEG_HTX_GRX_P14	C3	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_P14
PEG_GTX_C_HRX_N14	D11	PEG_RX#[1]	PEG_TX#[1]	E13	PEG_HTX_GRX_N14	C4	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_N14
PEG_GTX_C_HRX_P13	C10	PEG_RX[2]	PEG_TX[2]	G14	PEG_HTX_GRX_P13	C5	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_P13
PEG_GTX_C_HRX_N13	C9	PEG_RX#[2]	PEG_TX#[2]	G13	PEG_HTX_GRX_N13	C6	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_N13
PEG_GTX_C_HRX_P12	E10	PEG_RX[3]	PEG_TX[3]	F12	PEG_HTX_GRX_P12	C7	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_P12
PEG_GTX_C_HRX_N12	E9	PEG_RX#[3]	PEG_TX#[3]	F11	PEG_HTX_GRX_N12	C8	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_N12
PEG_GTX_C_HRX_P11	B8	PEG_RX[4]	PEG_TX[4]	J14	PEG_HTX_GRX_P11	C9	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_P11
PEG_GTX_C_HRX_N11	B7	PEG_RX#[4]	PEG_TX#[4]	J13	PEG_HTX_GRX_N11	C10	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_N11
PEG_GTX_C_HRX_P10	C6	PEG_RX[5]	PEG_TX[5]	D8	PEG_HTX_GRX_P10	C11	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_P10
PEG_GTX_C_HRX_N10	C5	PEG_RX#[5]	PEG_TX#[5]	D7	PEG_HTX_GRX_N10	C12	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_N10
PEG_GTX_C_HRX_P9	A5	PEG_RX[6]	PEG_TX[6]	D3	PEG_HTX_GRX_P9	C13	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_P9
PEG_GTX_C_HRX_N9	A6	PEG_RX#[6]	PEG_TX#[6]	C3	PEG_HTX_GRX_N9	C14	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_N9
PEG_GTX_C_HRX_P8	E2	PEG_RX[7]	PEG_TX[7]	E6	PEG_HTX_GRX_P8	C15	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_P8
PEG_GTX_C_HRX_N8	E1	PEG_RX#[7]	PEG_TX#[7]	E5	PEG_HTX_GRX_N8	C16	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_N8
PEG_GTX_C_HRX_P7	F4	PEG_RX[8]	PEG_TX[8]	F8	PEG_HTX_GRX_P7	C17	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_P7
PEG_GTX_C_HRX_N7	F3	PEG_RX#[8]	PEG_TX#[8]	E7	PEG_HTX_GRX_N7	C18	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_N7
PEG_GTX_C_HRX_P6	G2	PEG_RX[9]	PEG_TX[9]	G10	PEG_HTX_GRX_P6	C19	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_P6
PEG_GTX_C_HRX_N6	G1	PEG_RX#[9]	PEG_TX#[9]	G9	PEG_HTX_GRX_N6	C20	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_N6
PEG_GTX_C_HRX_P5	H3	PEG_RX[10]	PEG_TX[10]	G5	PEG_HTX_GRX_P5	C21	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_P5
PEG_GTX_C_HRX_N5	H4	PEG_RX#[10]	PEG_TX#[10]	G6	PEG_HTX_GRX_N5	C22	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_N5
PEG_GTX_C_HRX_P4	J1	PEG_RX[11]	PEG_TX[11]	K7	PEG_HTX_GRX_P4	C23	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_P4
PEG_GTX_C_HRX_N4	J2	PEG_RX#[11]	PEG_TX#[11]	K8	PEG_HTX_GRX_N4	C24	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_N4
PEG_GTX_C_HRX_P3	K3	PEG_RX[12]	PEG_TX[12]	J5	PEG_HTX_GRX_P3	C25	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_P3
PEG_GTX_C_HRX_N3	K4	PEG_RX#[12]	PEG_TX#[12]	J6	PEG_HTX_GRX_N3	C26	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_N3
PEG_GTX_C_HRX_P2	L1	PEG_RX[13]	PEG_TX[13]	M8	PEG_HTX_GRX_P2	C27	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_P2
PEG_GTX_C_HRX_N2	L2	PEG_RX#[13]	PEG_TX#[13]	M7	PEG_HTX_GRX_N2	C28	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_N2
PEG_GTX_C_HRX_P1	M3	PEG_RX[14]	PEG_TX[14]	L6	PEG_HTX_GRX_P1	C29	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_P1
PEG_GTX_C_HRX_N1	M4	PEG_RX#[14]	PEG_TX#[14]	L5	PEG_HTX_GRX_N1	C30	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_N1
PEG_GTX_C_HRX_P0	N1	PEG_RX[15]	PEG_TX[15]	N5	PEG_HTX_GRX_P0	C31	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_P0
PEG_GTX_C_HRX_N0	N2	PEG_RX#[15]	PEG_TX#[15]	N6	PEG_HTX_GRX_N0	C32	1	2	VGA@.1U_0402_16V7K PEG_HTX_C_GRX_N0

PEG

DMI_PTX_HRX_P0	W5	DMI_RX[0]	DMI_TX[0]
DMI_PTX_HRX_N0	W4	DMI_RX#[0]	DMI_TX#[0]
DMI_PTX_HRX_P1	V3	DMI_RX[1]	DMI_TX[1]
DMI_PTX_HRX_N1	V4	DMI_RX#[1]	DMI_TX#[1]
DMI_PTX_HRX_P2	Y3	DMI_RX[2]	DMI_TX[2]
DMI_PTX_HRX_N2	Y4	DMI_RX#[2]	DMI_TX#[2]
DMI_PTX_HRX_P3	AA4	DMI_RX_3	DMI_TX[3]
DMI_PTX_HRX_N3	AA5	DMI_RX#[3]	DMI_TX#[3]

DMI

			V7	DMI_HTX_PRX_P0	
			V6	DMI_HTX_PRX_N0	
			W7	DMI_HTX_PRX_P1	
			W8	DMI_HTX_PRX_N1	
			Y6	DMI_HTX_PRX_P2	
			Y7	DMI_HTX_PRX_N2	
			AA7	DMI_HTX_PRX_P3	
			AA8	DMI_HTX_PRX_N3	

	P3	PE_RX[0]	PE_TX[0]	P8	
	P4	PE_RX#[0]	PE_TX#[0]	P7	
	R2	PE_RX[1]	PE_TX[1]	R7	
	R1	PE_RX#[1]	PE_TX#[1]	R8	
	T1	PE_RX[2]	PE_TX[2]	T8	
	T2	PE_RX#[2]	PE_TX#[2]	T7	
	U2	PE_RX[3]	PE_TX[3]	U5	
	U1	PE_RX#[3]	PE_TX#[3]	U6	

GEN

7/20 PE_RX[0~3]/PE_RX#[0~3] only use on Workstation.

7/20 PE_TX[0~3]/PE_TX#[0~3] only use on Workstation.

+1.05VCCIO

24.9_0402_1% 2 — 1 R1 PEG_IRCOMP B5

PEG_ICOMPO	B5	
PEG_RCOMPO	C4	
PEG_ICOMPI	B4	

LOTES_ACAZIF096P01_SANDYBRIDGE 3 OF 11 CONN@

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - ;Width/Space= (4 mils/15mils)
PEG_ICOMPO signals should be routed with - max length = 500 mils - Width/Space (12 mils/15mils)

1000P_0402_50V7K @ 2 — 1 C1007 H_FDI_FSYNC0
1000P_0402_50V7K @ 2 — 1 C1008 H_FDI_LSYNC0
1000P_0402_50V7K @ 2 — 1 C1009 H_FDI_FSYNC1
1000P_0402_50V7K @ 2 — 1 C1010 H_FDI_LSYNC1
1000P_0402_50V7K @ 2 — 1 C1011 H_FDI_INT

8/23 Add

H_FDI_TXN[0..7] 16
H_FDI_TXP[0..7] 16

JCPU1D SKT_H2

16 H_FDI_FSYNC0 — AC5 FDI_FSYNC_0
16 H_FDI_LSYNC0 — AC4 FDI_LSYNC_0

16 H_FDI_FSYNC1 — AE5 FDI_FSYNC_1
16 H_FDI_LSYNC1 — AE4 FDI_LSYNC_1

+1.05VCCIO
16 H_FDI_INT — AG3 FDI_INT
24.9_0402_1% 2 — 1 R2 FDI_ICOMP AE2 FDI_COMPIO
AE1 FDI_ICOMPO

FDI_TX[0]

FDI_TX[0]	AC8	H_FDI_TXP0	FDI_TX[4]	AD7	H_FDI_TXP4
FDI_TX#[0]	AC7	H_FDI_TXN0	FDI_TX#[4]	AD6	H_FDI_TXN4
FDI_TX[1]	AC2	H_FDI_TXP1	FDI_TX[5]	AE7	H_FDI_TXP5
FDI_TX#[1]	AC3	H_FDI_TXN1	FDI_TX#[5]	AE8	H_FDI_TXN5
FDI_TX[2]	AD2	H_FDI_TXP2	FDI_TX[6]	AF3	H_FDI_TXP6
FDI_TX#[2]	AD1	H_FDI_TXN2	FDI_TX#[6]	AF2	H_FDI_TXN6
FDI_TX[3]	AD4	H_FDI_TXP3	FDI_TX[7]	AG2	H_FDI_TXP7
FDI_TX#[3]	AD3	H_FDI_TXN3	FDI_TX#[7]	AG1	H_FDI_TXN7

FDI LINK

LOTES_ACAZIF096P01_SANDYBRIDGE 4 OF 11 CONN@

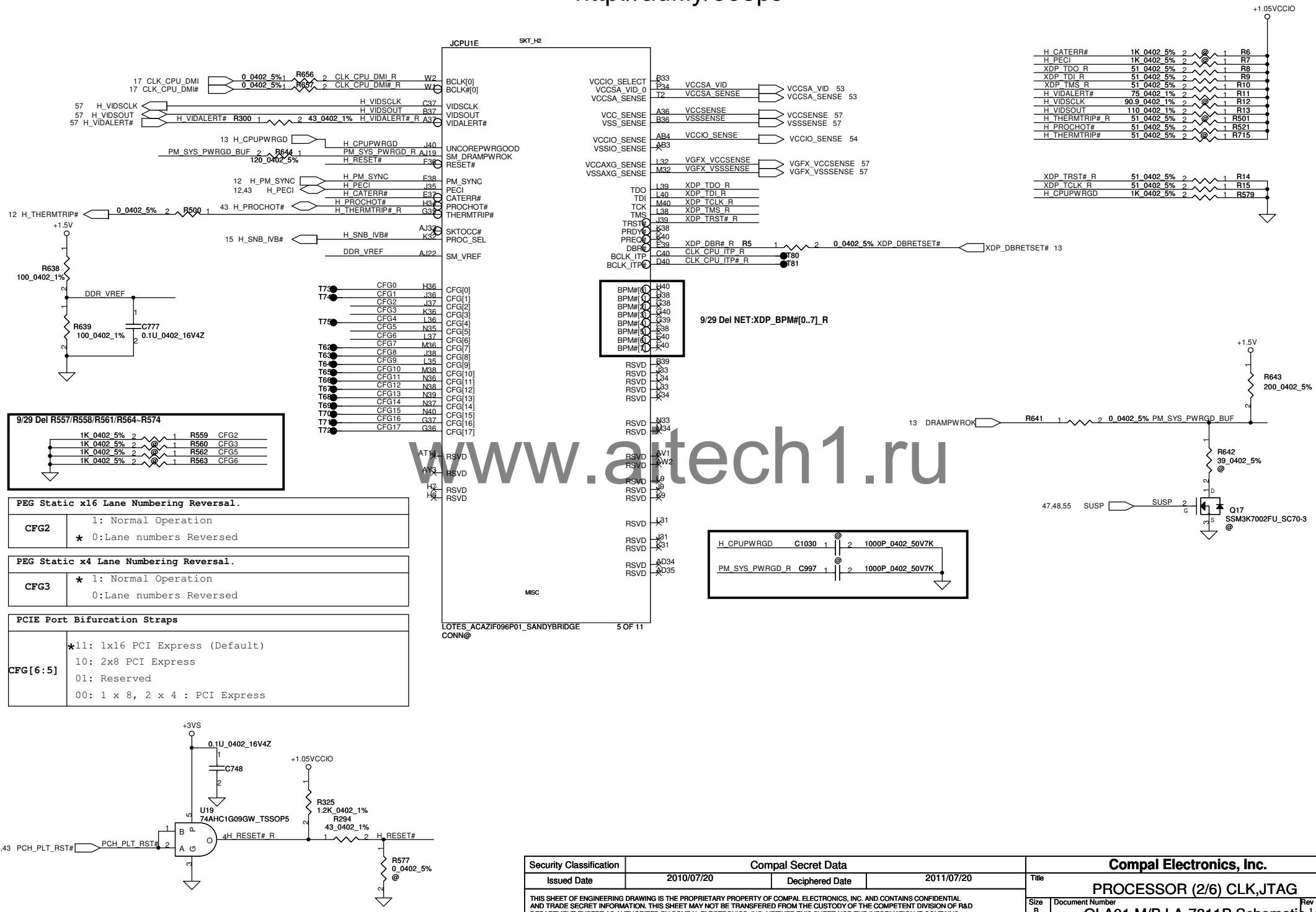
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PROCESSOR (1/6) DMI,FDI,PEG

Size	Document Number	Rev
B	QLA01 M/B LA-7811P Schematic	1.A

Date: Thursday, June 16, 2011 Sheet 4 of 63



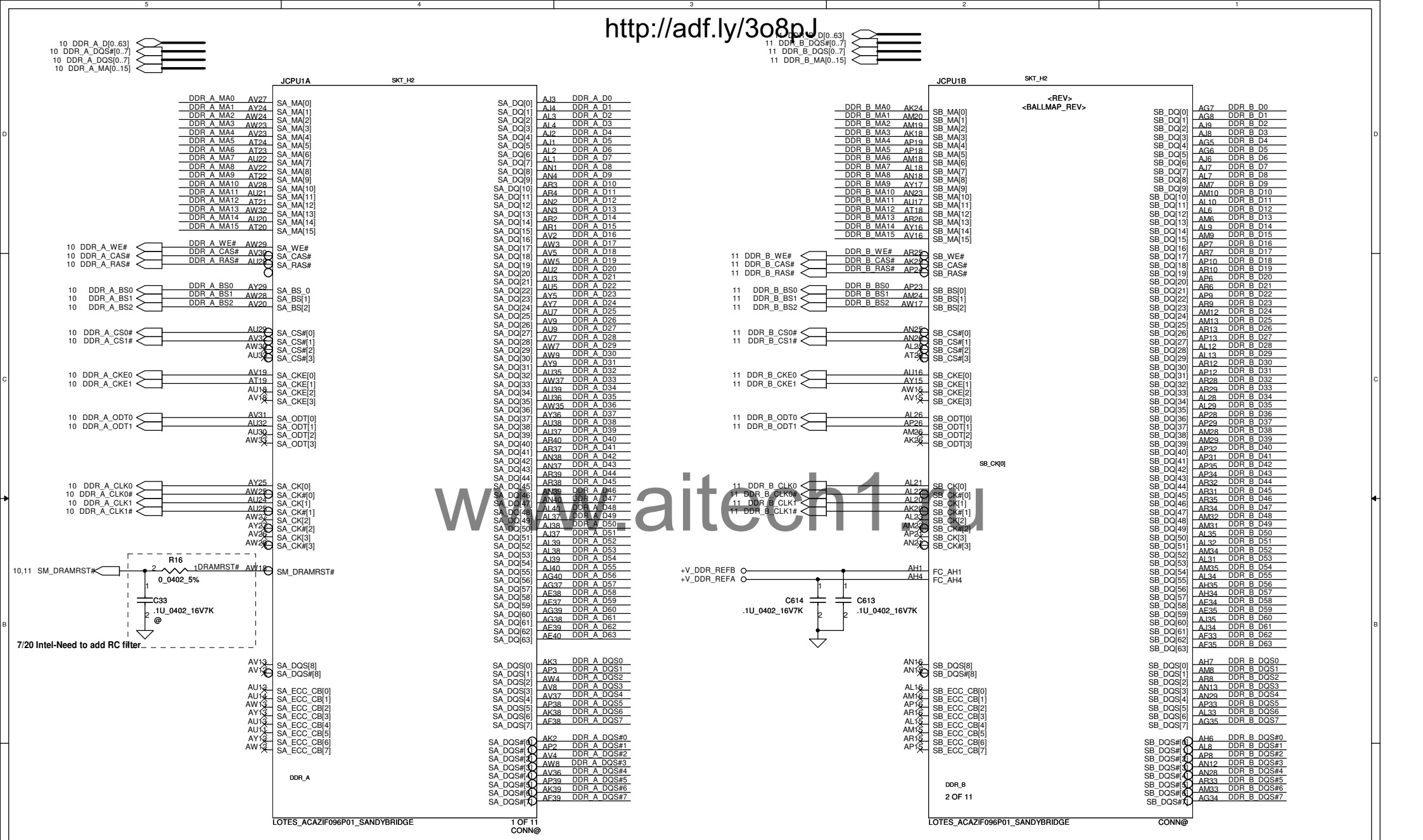
PEG Static x16 Lane Numbering Reversal.	
CFG2	1: Normal Operation * 0:Lane numbers Reversed

PEG Static x4 Lane Numbering Reversal.	
CFG3	* 1: Normal Operation 0:Lane numbers Reversed

PCIE Port Bifurcation Straps	
CFG[6:5]	*11: 1x16 PCI Express (Default) 10: 2x8 PCI Express 01: Reserved 00: 1 x 8, 2 x 4 : PCI Express

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.			
Title	PROCESSOR (2/6) CLK,JTAG		
Size B	Document Number QLA01 M/B LA-7811P Schematic		Rev 1.A
Date: Thursday, June 16, 2011		Sheet 5 of 63	

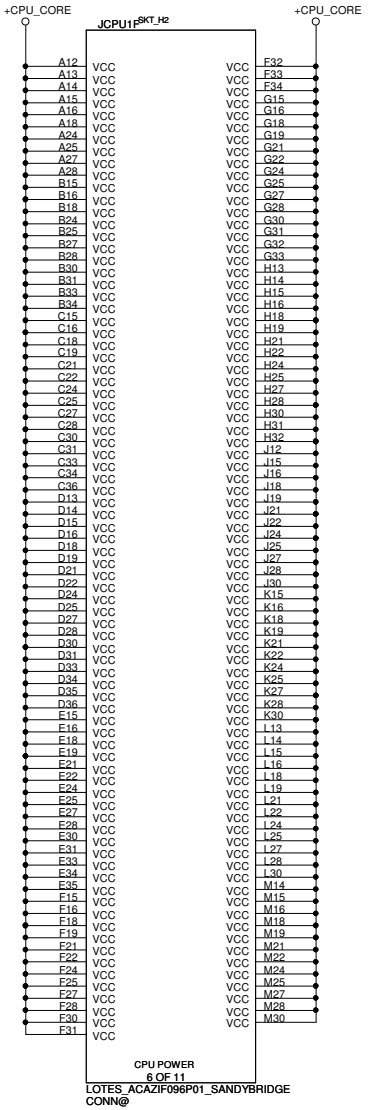


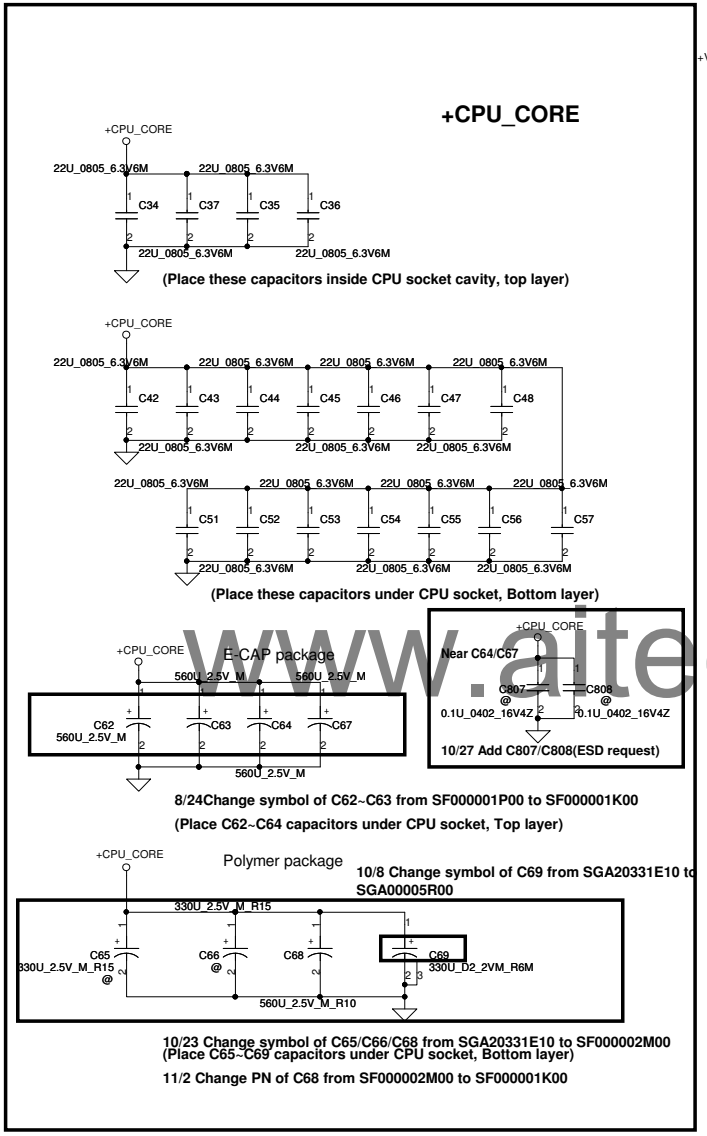
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

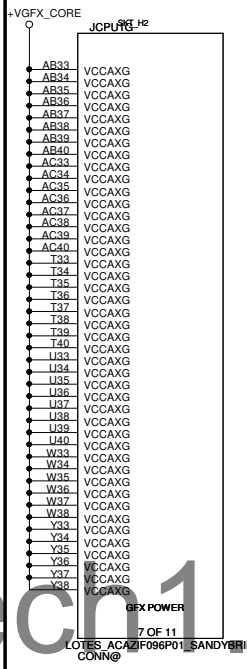
Title	PROCESSOR (3/6) DDRIII	
Size B	Document Number QLA01 M/B LA-7811P Schematic	Rev 1.A
Date: Thursday, June 16, 2011	Sheet 6 of 63	

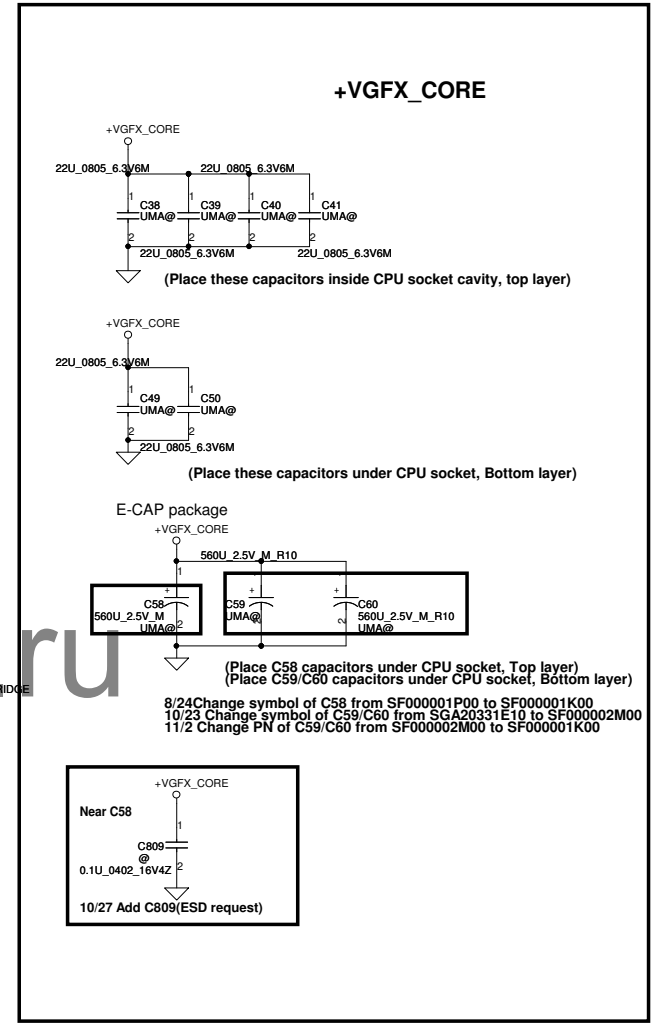
+CPU_CORE:112A





+VGFX_CORE:35A





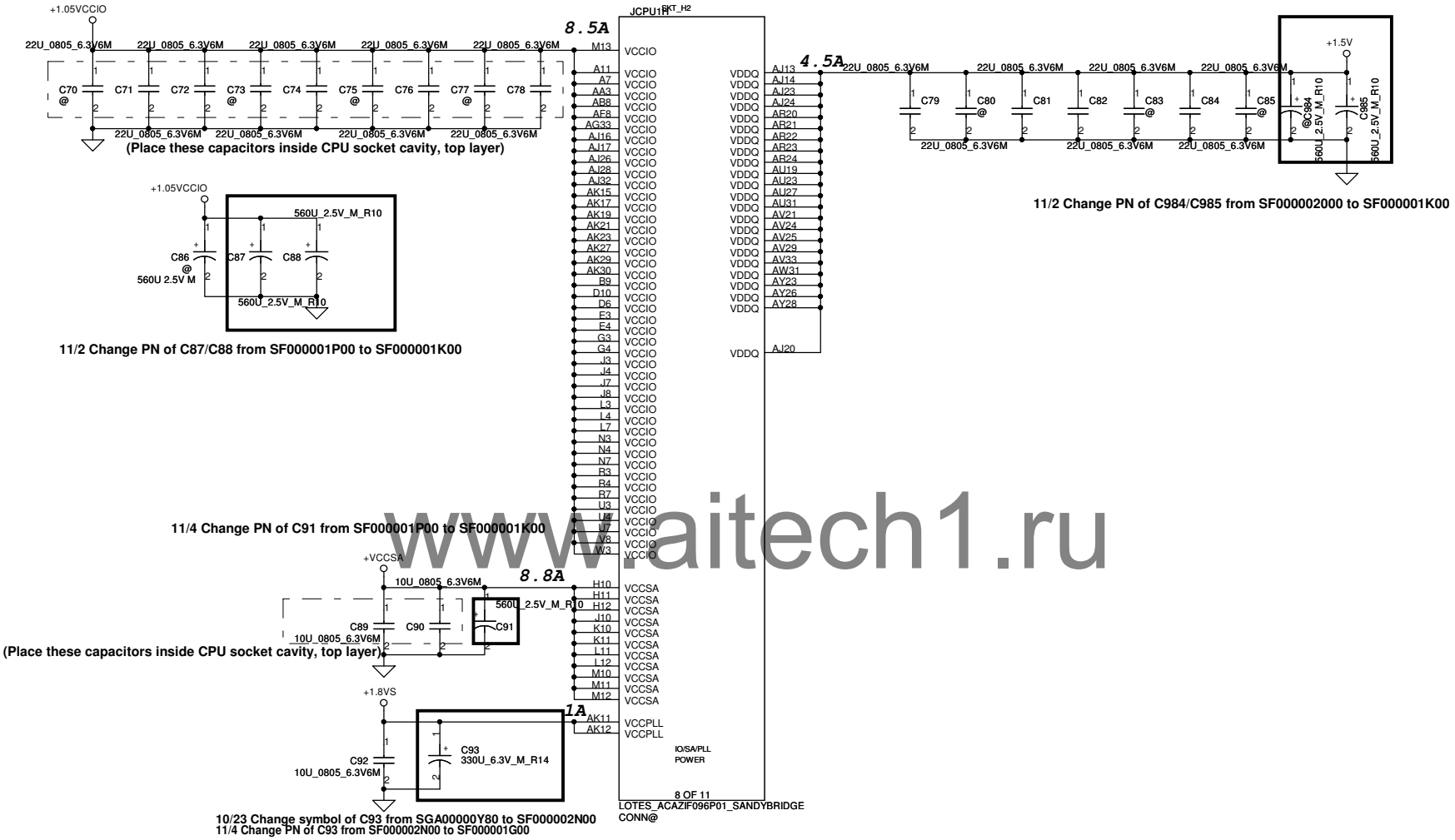
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PROCESSOR (4/6) PWR,Bypass

Size: Custom | Document Number: QLA01 M/B LA-7811P Schematic | Rev: 1.A

Date: Thursday, June 09, 2011 | Sheet 7 of 63



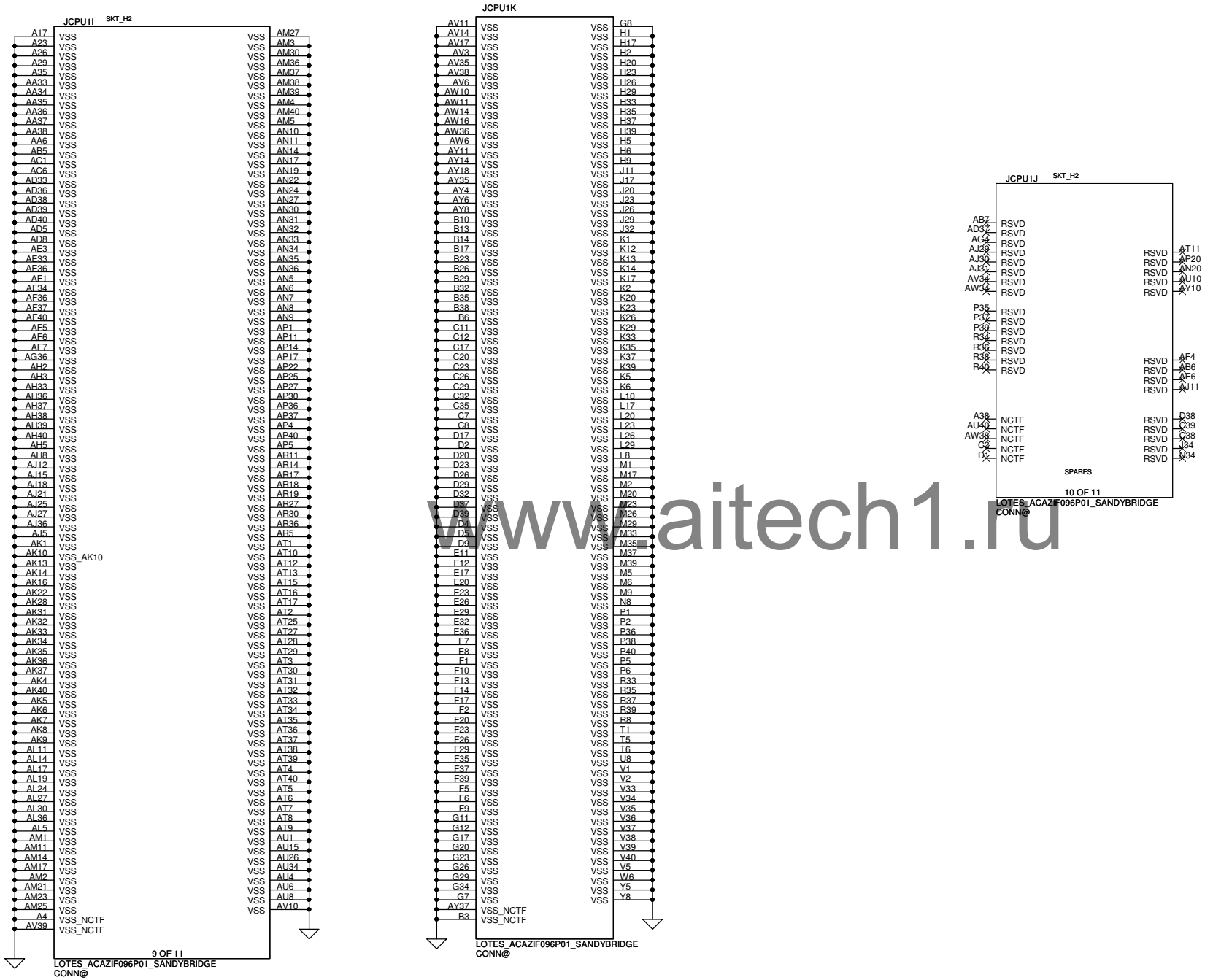
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PROCESSOR (5/6) PWR

Size	Document Number	Rev
Custom	QLA01 M/B LA-7811P Schematic	1.A

Date: Thursday, June 09, 2011 Sheet 8 of 63



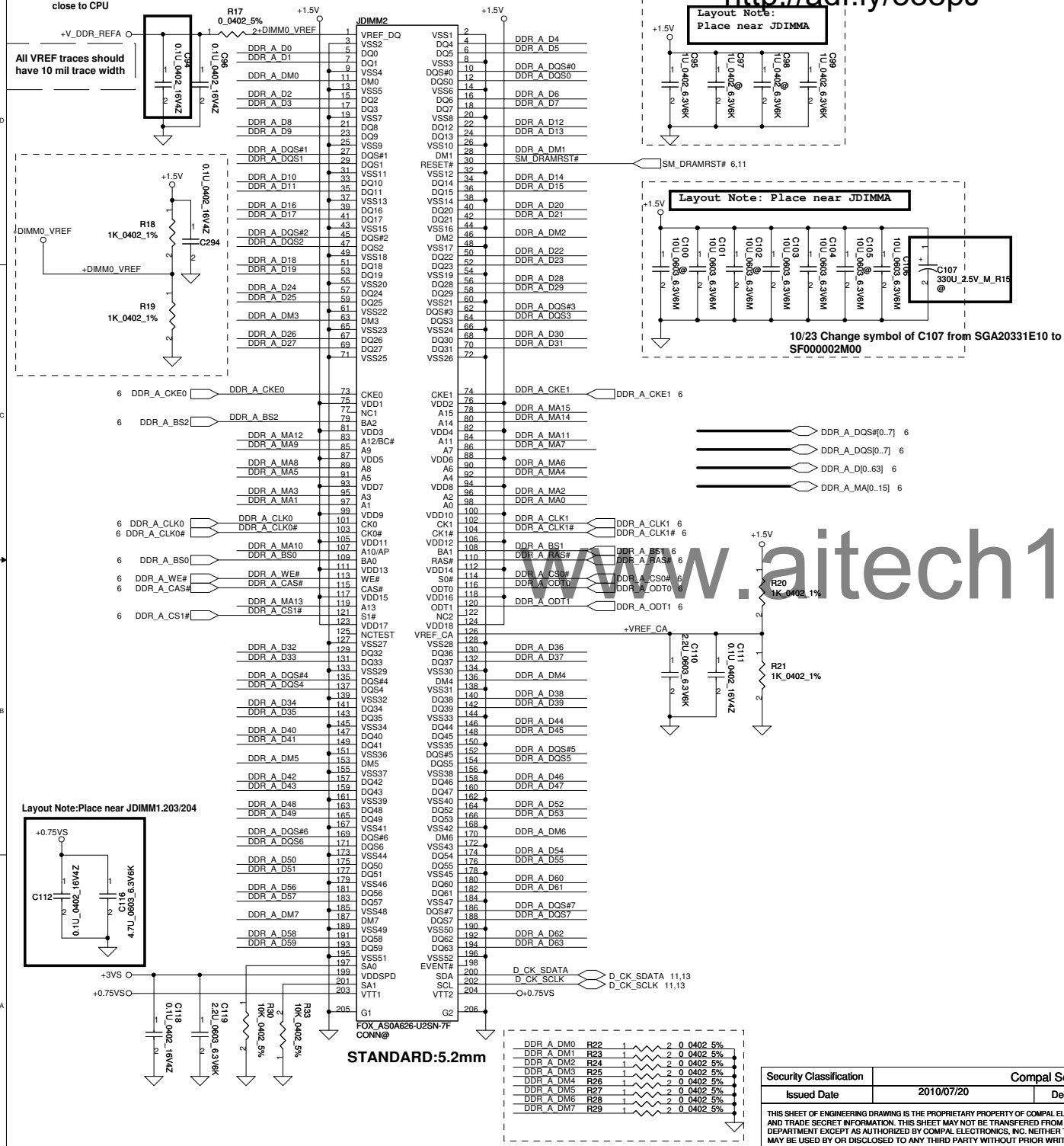
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PROCESSOR (6/6) VSS

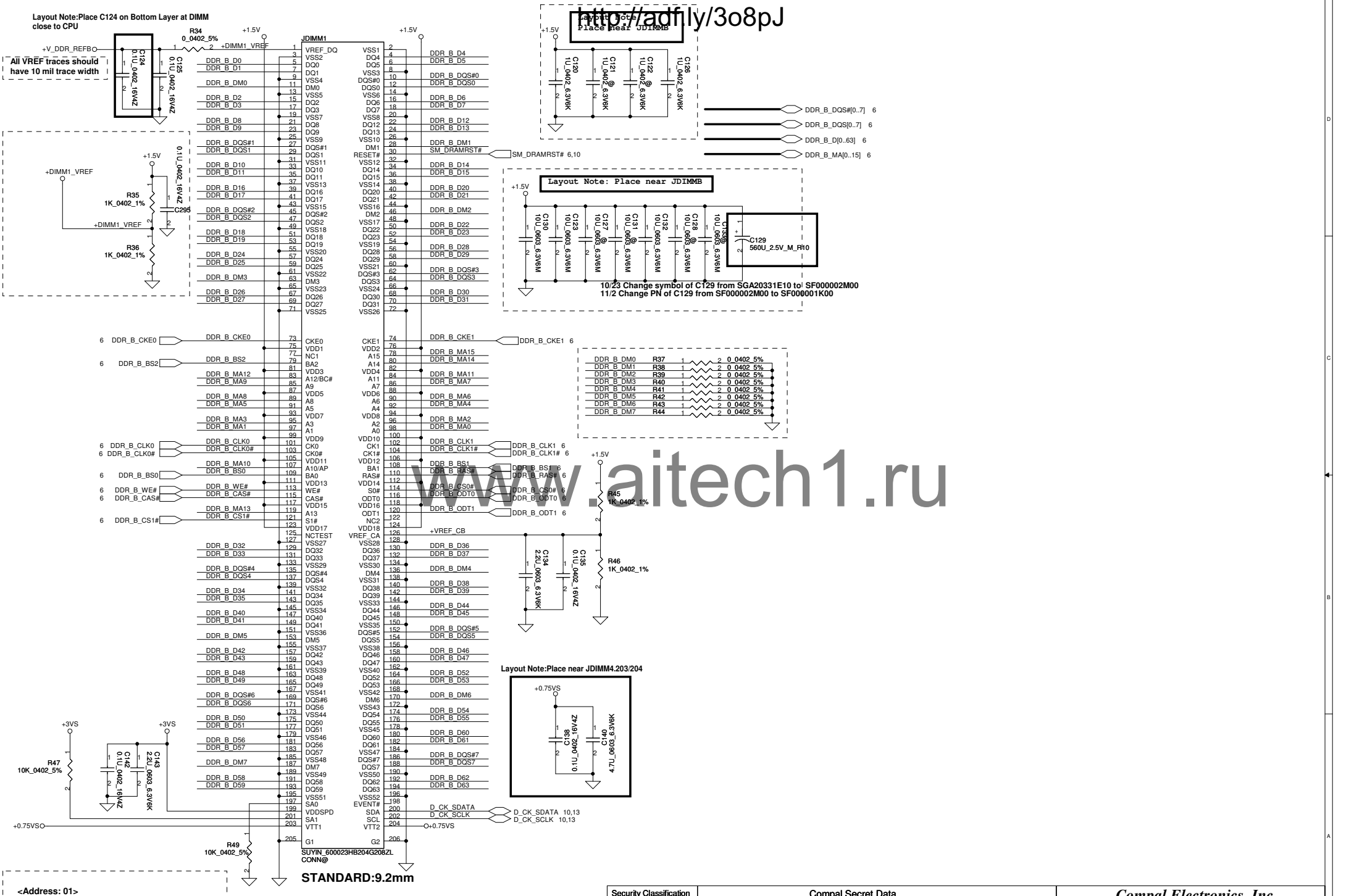
Size	Document Number	Rev
Custom	QLA01 M/B LA-7811P Schematic	1.A

Date: Thursday, June 09, 2011 Sheet 9 of 63



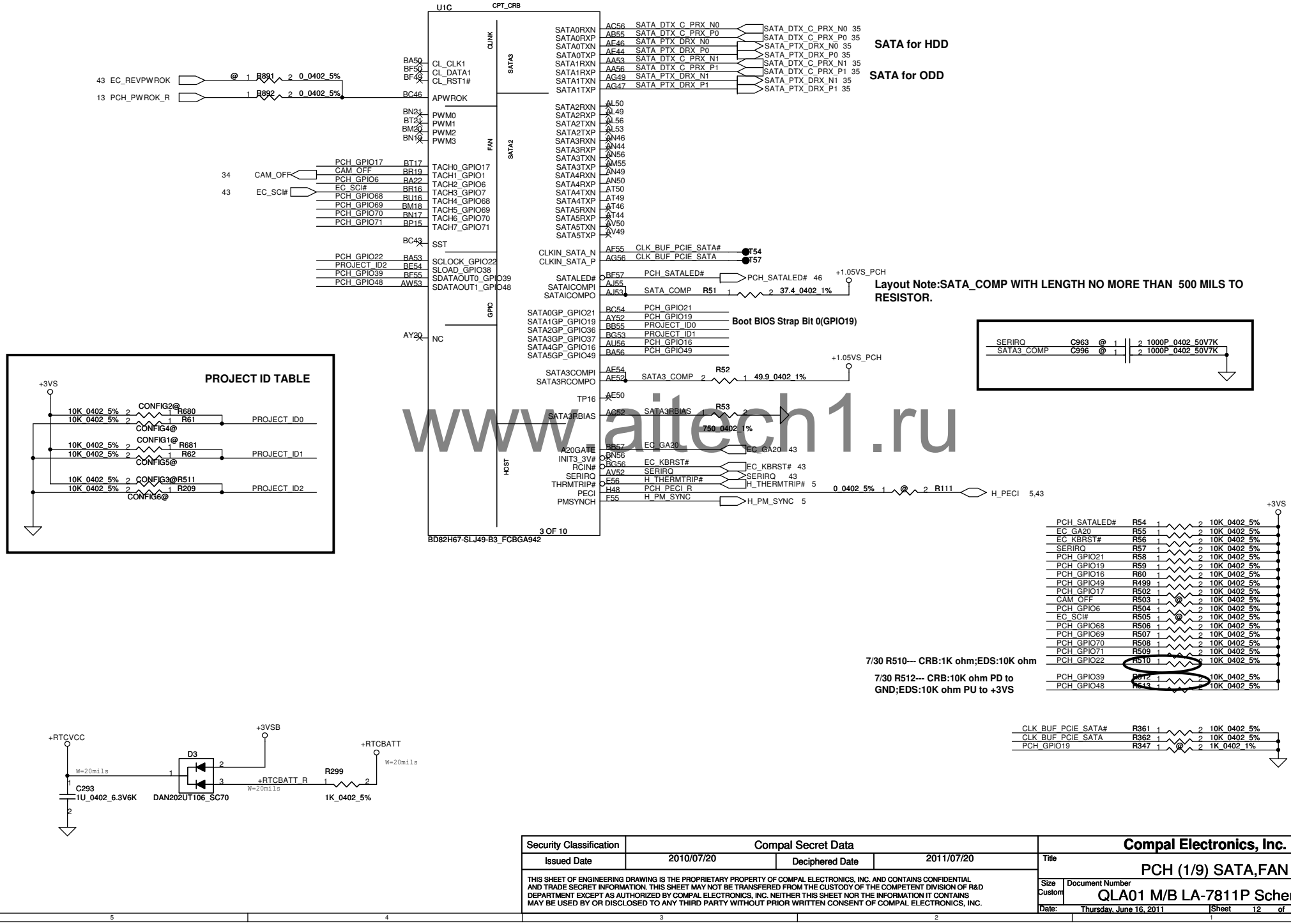
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.	
Title	DDRIII CHANNELA
Size: Custom	Document Number: QLA01 M/B LA-7811P Schematic
Rev	1.A
Date: Thursday, June 16, 2011	Sheet 10 of 63



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.		
Title	DDRIII CHANNELB	
Size: Custom	Document Number: QLA01 M/B LA-7811P Schematic	Rev: 1.A
Date: Thursday, June 16, 2011	Sheet 11 of 63	



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PCH (1/9) SATA,FAN

Size	Document Number	Rev
Custom	QLA01 M/B LA-7811P Schematic	1.A
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HDA for AUDIO

39 HDA_BITCLK_AUDIO — R69 33_0402_5% — HDA_BITCLK_PCH
39 HDA_RST#_AUDIO — R72 33_0402_5% — HDA_RST#_PCH
39 HDA_SDOUT_AUDIO — R73 33_0402_5% — HDA_SDOUT_PCH

HDA_SDO
ME debug mode,
this signal has a weak internal pull down
*Low = Disable (default)
High = Enable (flash descriptor security overide)

HDA_SYNC
This signal has a weak internal pull down
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V
*Need to pull high for Huron River platform

39 HDA_SYNC_AUDIO — R70 33_0402_5% — HDA_SYNC_AUDIO_R
@ R356 1M_0402_5%

PCH_RSMRST# R303 0_0402_5% PCH_DPWROK
Stuff R303 if do not support DeepSX state

EC_PWROK R344 0_0402_5% PCH_PWROK_R

U1D

LDRQ1#_GPIO23	BA20	43 LPC_AD0
FWH0_LAD0	BK15	43 LPC_AD1
FWH1_LAD1	BJ17	43 LPC_AD2
FWH2_LAD2	BJ20	43 LPC_AD3
FWH3_LAD3	BG20	
LDRQ0#	BK17	43 LPC_FRAME#
FWH4_LFRAME#	BG17	
HDA_BCLK	BU22	HDA_BITCLK_PCH
HDA_RST#	BC22	HDA_RST# PCH
HDA_SDIN0	BD22	HDA_SDIN0
HDA_SDIN1	BF22	39 HDA_SDIN0
HDA_SDIN2	BK22	+3VALW R338 2 @ 1 1K_0402_1%
HDA_SDIN3	BJ22	
HDA_SDO	BT23	43 ME_FLASH R890 0_0402_5% HDA_SDOUT_PCH
HDA_SYNC	BP23	HDA_SYNC_AUDIO_R
SPI_MOSI	AU53	PCH_SPI_MOSI_1 R79 0_0402_5% PCH_SPI_MOSI
SPI_MISO	AT55	PCH_SPI_MISO_1 R80 0_0402_5% PCH_SPI_MISO
SPI_CS0#	AT57	PCH_SPI_CS0# R81 0_0402_5% PCH_SPI_CS0#_R
SPI_CLK	AR54	PCH_SPI_CLK_1 R83 0_0402_5% PCH_SPI_CLK
SPI_CS1#	AR56	

+3VALW
2.2K_0402_5% R945 PCH_SMBCLK
2.2K_0402_5% R946 PCH_SMBDATA

RTCX1	BR39	PCH_RTCX1
RTCX2	BN39	PCH_RTCX2
RTCRST#	BT41	PCH_RTCRST#
SRTCRST#	BN37	PCH_SRTCRST#
INTRUDER#	BM38	SM_INTRUDER#
PWROK	BJ38	12 PCH_PWROK_R
RSMRST#	BK38	PCH_RSMRST#
INTVRMEN	BN41	PCH_INTVRMEN
DPWROK	BT37	PCH_DPWROK
DSWVRMEN	BR42	PCH_DSWVRMEN

SMBALERT#_GPIO11	BN49	PCH_GPIO11
SMBCLK	BT47	42 PCH_SMBCLK
SMBDATA	BR49	42 PCH_SMBDATA
SML0ALERT#_GPIO60	BU49	PCH_GPIO60
SML0CLK	BT51	LAN_SMBCLK
SML0DATA	BM50	LAN_SMBDATA
SML1ALERT# PCHHOT#_GPIO74	BR46	PCH_GPIO74
SML1CLK_GPIO58	BJ46	PCH_SML1CLK
SML1DATA_GPIO75	BK46	PCH_SML1DAT

BMBUSY#_GPIO0	AW55	PCH_GPIO0
CLKRUN#_GPIO32	BC56	CLKRUN# 43
HDA_DOCK_EN#_GPIO33	BC25	PCH_GPIO33
STP_PCI#_GPIO34	BL56	PCH_GPIO34
GPIO35	BJ57	PCH_GPIO35
GPIO8	BP51	EC_SMI# 36,43
LAN_PHY_PWR_CTRL_GPIO12	BK50	PM_LANPHY_ENABLE
HDA_DOCK_RST#_GPIO13	BA25	PCH_GPIO13
GPIO15	BM55	SMIB 36
GPIO24_MEM_LED	BP53	T1
GPIO28	BJ55	PCH_GPIO28
SLP_LAN#_GPIO29	BH49	SLP_LAN# 38
PCIECLKRQ2#_GPIO20	AV43	LAN_CLKREQ# 38
PCIECLKRQ5#_GPIO44	BL54	WLAN_CLKREQ# 42
PCIECLKRQ6#_GPIO45	AV44	CLKREQ_USB30# 36
PCIECLKRQ7#_GPIO46	BP55	TV_CLKREQ# 42
GPIO57	BT53	PCH_GPIO57
SYS_PWROK	BJ53	SYS_PWROK_R
RI#	BJ48	EC_SWI# 43
PLTRST#	BK48	PCH_PLT_RST# 5,38,43
WAKE#	BC44	PCH_PCIE_WAKE# R R364 0_0402_5% PCH_PCIE_WAKE# 36,38,42
SLP_A#	BC41	
SLP_S3#	BM53	PM_SLP_S3# 43
SLP_S4#	BN52	PM_SLP_S4# 43
SLP_S5#_GPIO63	BH50	PM_SLP_S5# 43
SUS_STAT#_GPIO61	BN54	T2
SUSCLK_GPIO62	BA47	PCH_SUSCLK_R R363 0_0402_5% PCH_SUSCLK 43
BATLOW#_GPIO72	AV46	PCH_GPIO72
SUSACK#	BP45	SUS_PWR_ACK_R R365 0_0402_5% SUS_PWR_ACK 43
SUSWARN#-SUS_PWR_DN_ACK-GPIO30	BU46	SUSWARN#_R R390 0_0402_5% SUSWARN# 43
DRAMPWROK	BG46	DRAMPWROK 5
GPIO27	BJ43	PCH_GPIO27
GPIO31	BG43	PCH_GPIO31
SLP_SUS#	BD43	T51
PWRBTN#	BT43	PBTN_OUT# 43
SYS_RESET#	BE52	XDP_DBRETSET# 5
SPKR	BE56	PCH_SPKR 39
PROCPWRGD	D53	H_CPUPWRGD 5

TP12	BC49	PCH_JTAG_RST#
JTAG_TCK	BA43	PCH_JTAG_TCK
JTAG_TDI	BC52	PCH_JTAG_TDI
JTAG_TDO	BF47	PCH_JTAG_TDO
JTAG_TMS	BC50	PCH_JTAG_TMS

4 OF 10
BD82H67-SLJ49-B3_FCBGA942

+3VALW
EC_SMI# R324 10K_0402_5%
EC_SWI# R74 10K_0402_5%
PCH_GPIO74 R75 10K_0402_5%
PCH_SML1CLK R63 4.7K_0402_5%
PCH_SML1DAT R76 4.7K_0402_5%
LAN_SMBCLK R64 2.2K_0402_5%
LAN_SMBDATA R65 2.2K_0402_5%
PCH_GPIO60 R77 2.2K_0402_5%
PM_LANPHY_ENABLE R66 @ 10K_0402_5%
SMIB R67 10K_0402_5%
PCH_GPIO28 R68 1K_0402_1%
PCH_GPIO13 R896 10K_0402_5%
SUSWARN#_R R448 10K_0402_5%
PCH_GPIO57 R71 10K_0402_5%
PCH_GPIO27 R78 10K_0402_5%
WLAN_CLKREQ# R530 10K_0402_5%
CLKREQ_USB30# R531 10K_0402_5%
TV_CLKREQ# R532 10K_0402_5%
DRAMPWROK R646 @ 200_0402_5%
PCH_GPIO31 R675 10K_0402_5%
PCH_GPIO72 R676 200_0402_5%
PCH_PCIE_WAKE# R R203 1K_0402_1%
PCH_GPIO11 R716 10K_0402_5%

Stuff R391 if EC don't want to involve in the handshake mechanism for the DeepSX state entry and exit

+3VS
PCH_GPIO33 R894 10K_0402_5%
PCH_GPIO0 R82 10K_0402_5%
PCH_GPIO34 R84 10K_0402_5%
LAN_CLKREQ# R529 10K_0402_5%
XDP_DBRETSET# R581 10K_0402_5%
PCH_SPKR R583 @ 1K_0402_5%
PCH_SPKR:HIGH= Enable (No Reboot);
* LOW= Disable(Default)

CLKRUN# R926 @ 10K_0402_5%
SLP_LAN# R897 @ 1K_0402_1%
PCH_GPIO33 R895 @ 1K_0402_1%
SYS_PWROK R719 @ 10K_0402_5%
PCH_GPIO35 R85 @ 2.2K_0402_5%
EC_SMI# R86 @ 1K_0402_1%
SUSWARN#_R R207 @ 1K_0402_1%
EC_PWROK R718 @ 10K_0402_5%
PCH_GPIO28 R340 @ 1K_0402_1%
* On-Die PLL Voltage Regulator
H: Enable
L: Disable

XDP_DBRETSET# C676 @ 0.1U_0402_16V4Z <EMI>
8/13 Add C676 close to U1(EMI request)

C146 18P_0402_50V8J
X1 32.768KHZ_12.5PF_Q13MC14610002
C147 18P_0402_50V8J
PCH_RTCX1 — R87 10M_0402_5% — PCH_RTCX2

8/20 Add
1000P_0402_50V7K C987 LAN_CLKREQ#
1000P_0402_50V7K C988 PCH_JTAG_TDO

+RTCVCC close to RAM door R99 20K_0402_1% PCH_SRTCRST#
J2 10K_0603_5% C149 1U_0402_6.3V6K RC Delay 18~25mS

+3VS R655 4.7K_0402_5% — PCH_SMBCLK — Q32 SSM3K7002FU_SC70-3 — D_CK_SCLK — D_CK_SCLK 10,11
+3VS R654 4.7K_0402_5% — PCH_SMBDATA — Q31 SSM3K7002FU_SC70-3 — D_CK_SDATA — D_CK_SDATA 10,11

+3VS R94 4.7K_0402_5% SPI_WP1# R96 4.7K_0402_5% SPI_HOLD1#
U2 SA000041P00 4MB
CS# VCC PCH_SPI_CS0# — PCH_SPI_CLK_1
WP# SCLK — PCH_SPI_MOSI_1
HOLD# SI — PCH_SPI_MISO_1
GND SO
S IC FL 32M MX25L3206EM2I-12G SOP 8P
SPI ROM Footprint 200mil

8/19 Change footprint of U2 to WIESO_G6179-100000_8P

+RTCVCC close to RAM door R90 20K_0402_1% PCH_RTCRST#
J1 10K_0603_5% C148 1U_0402_6.3V6K RC Delay 18~25mS

R348 @ 0_0402_5%
+3VS
U20 NC7SZ08P5X_NL_SC70-5
SYS_PWROK — EC_PWROK — EC_PWROK 43
VGATE — VGATE 43,57

R342 @ 0_0402_5%
Q18 MMBT3906_SOT23-3
PCH_RSMRST# — EC_RSMRST# 43
R717 10K_0402_5%
R319 4.7K_0402_5% — +3VALW
D38A BAV99DW-7-F_SOT363~N
D38B BAV99DW-7-F_SOT363~N
R343 2.2K_0402_5%

+3VALW
PCH_JTAG_TMS — R91 200_0402_5% R92 100_0402_5%
PCH_JTAG_TDO — R93 200_0402_5% R95 100_0402_5%
PCH_JTAG_TDI — R97 200_0402_5% R98 100_0402_5%
PCH_JTAG_RST# — R100 20K_0402_5% R101 10K_0402_5%
PCH_JTAG_TCK — R102 51_0402_5%

+RTCVCC
1M_0402_5% R103 SM_INTRUDER#
390K_0402_5% R104 PCH_DSWVRMEN
390K_0402_5% R105 PCH_INTVRMEN
R106 1K_0402_5% @

R943 0_0402_5%
+3VS
@ U25 NC7SZ08P5X_NL_SC70-5
PCH_PLT_RST# — PLT_RST# — PLT_RST# 22,36,37,42
R944 100K_0402_5%

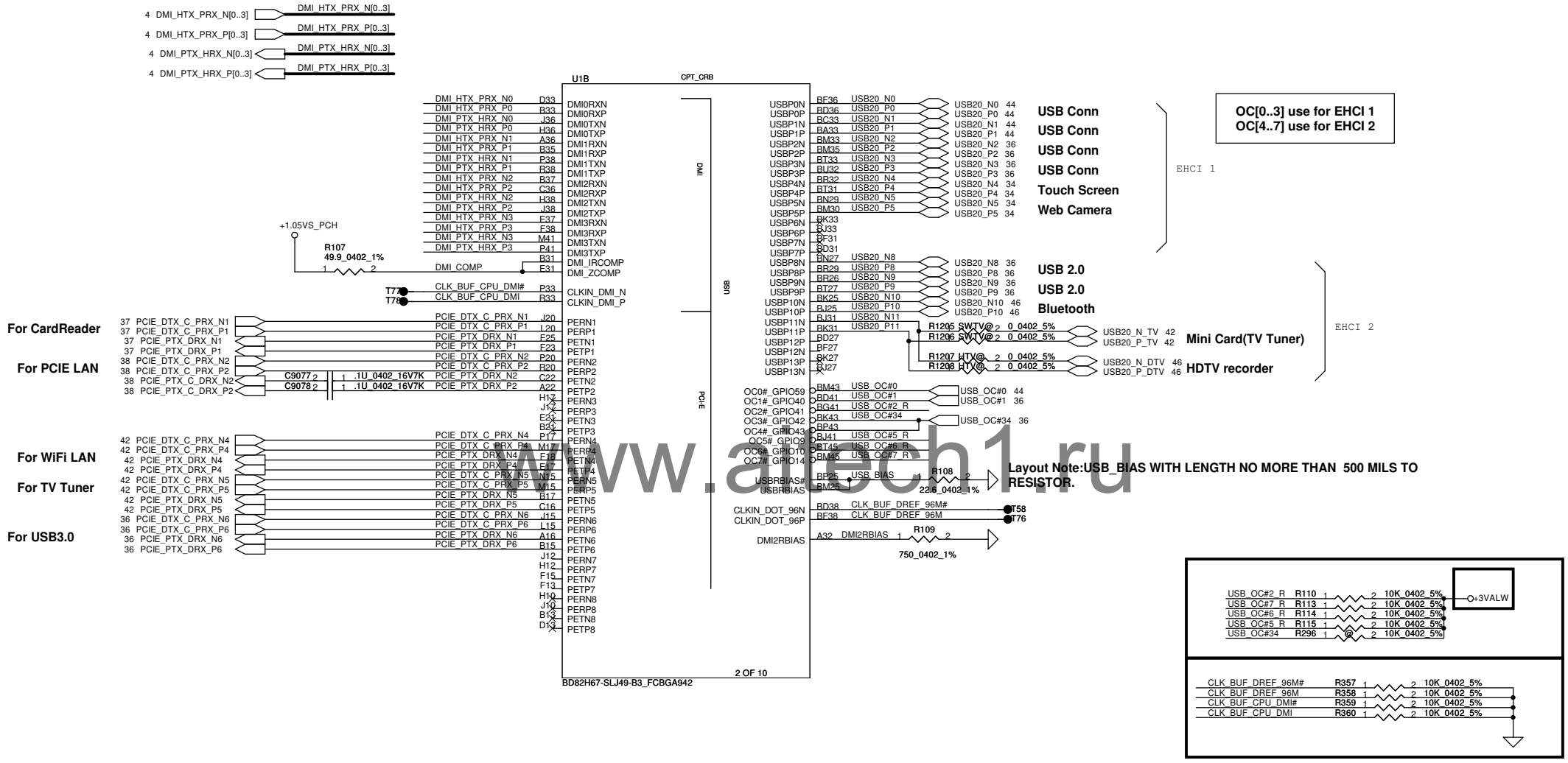
SYS_PWROK_R — R349 0_0402_5% — SYS_PWROK
R350 @ 0_0402_5% — VGATE

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

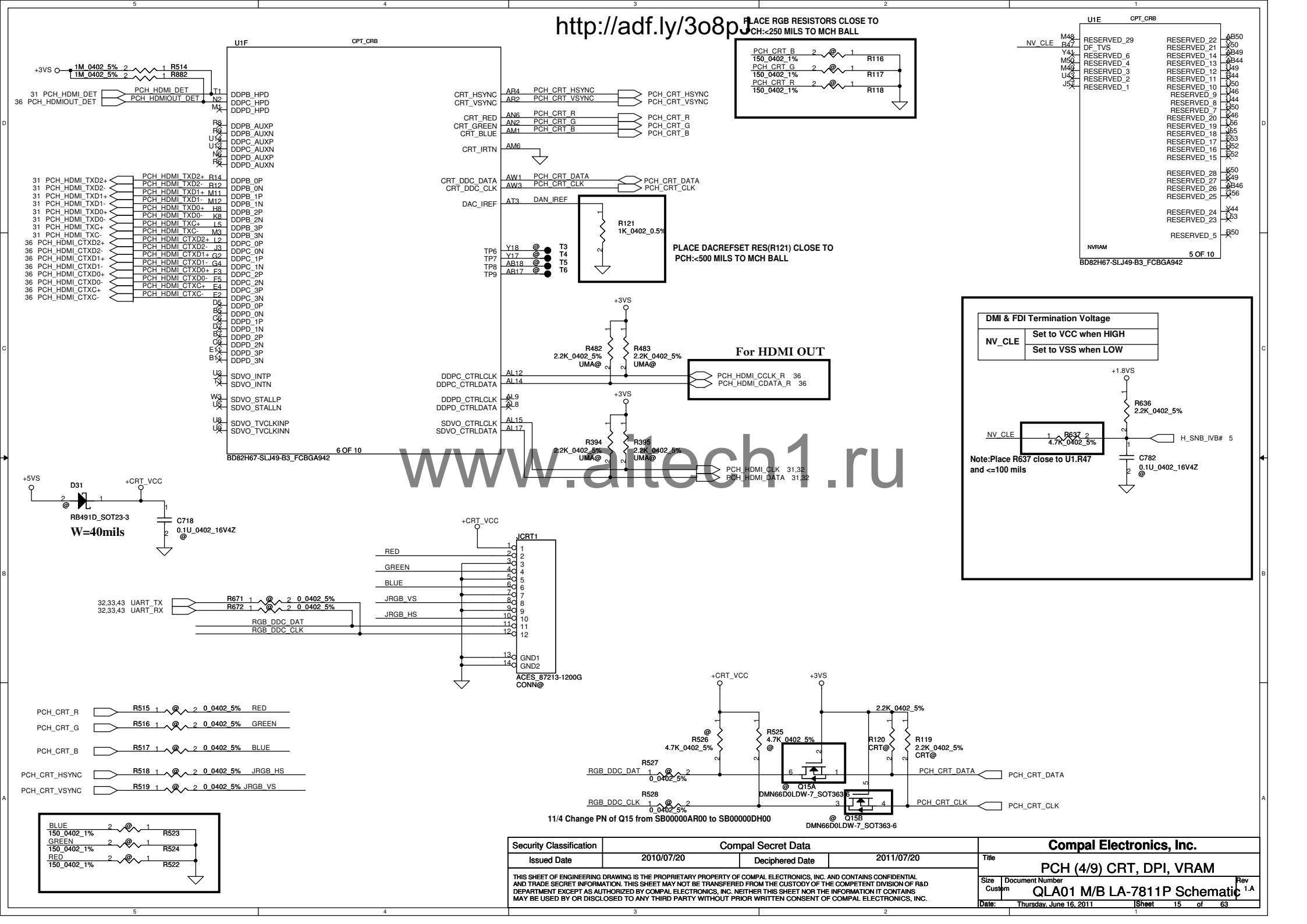
Title: PCH (2/9) LPC, HDA, SMBUS

Size	Document Number	Rev
Custom	QLA01 M/B LA-7811P Schematic	1.A
Date: Thursday, June 16, 2011	Sheet 13 of 63	



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.			
Title	PCH (3/9) DMI, USB, PCIE		
Size A	Document Number QLA01 M/B LA-7811P Schematic		Rev 1.A
Date: Thursday, June 16, 2011	Sheet 14 of 63		



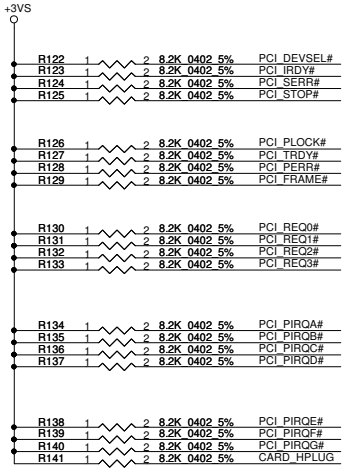
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

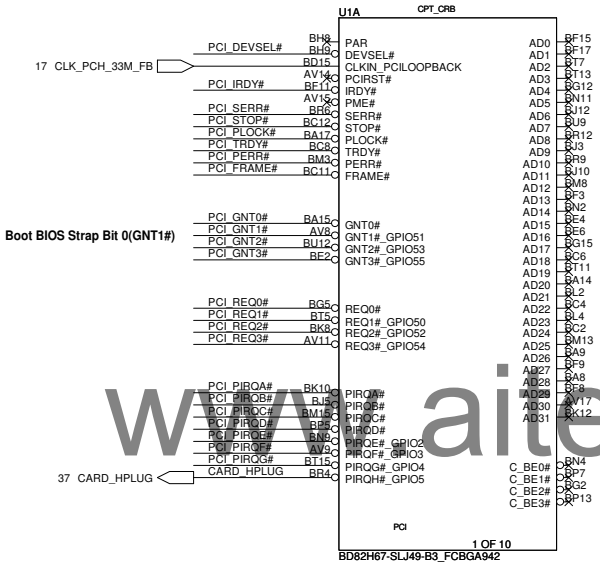
Compal Electronics, Inc.

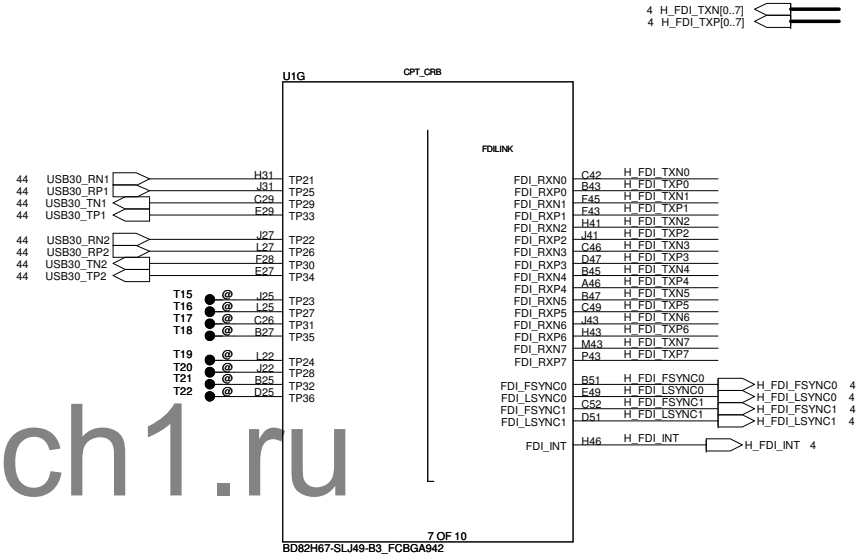
Title: PCH (4/9) CRT, DPI, VRAM

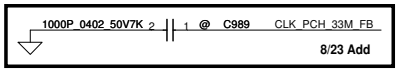
Size	Document Number	Rev
Custom	QLA01 M/B LA-7811P Schematic	1.A

Date: Thursday, June 16, 2011 Sheet 15 of 63

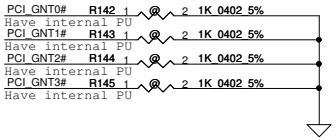








Boot BIOS Strap		
PCH_GNT1#	PCH_GPIO19	Boot BIOS Loaction
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI ★



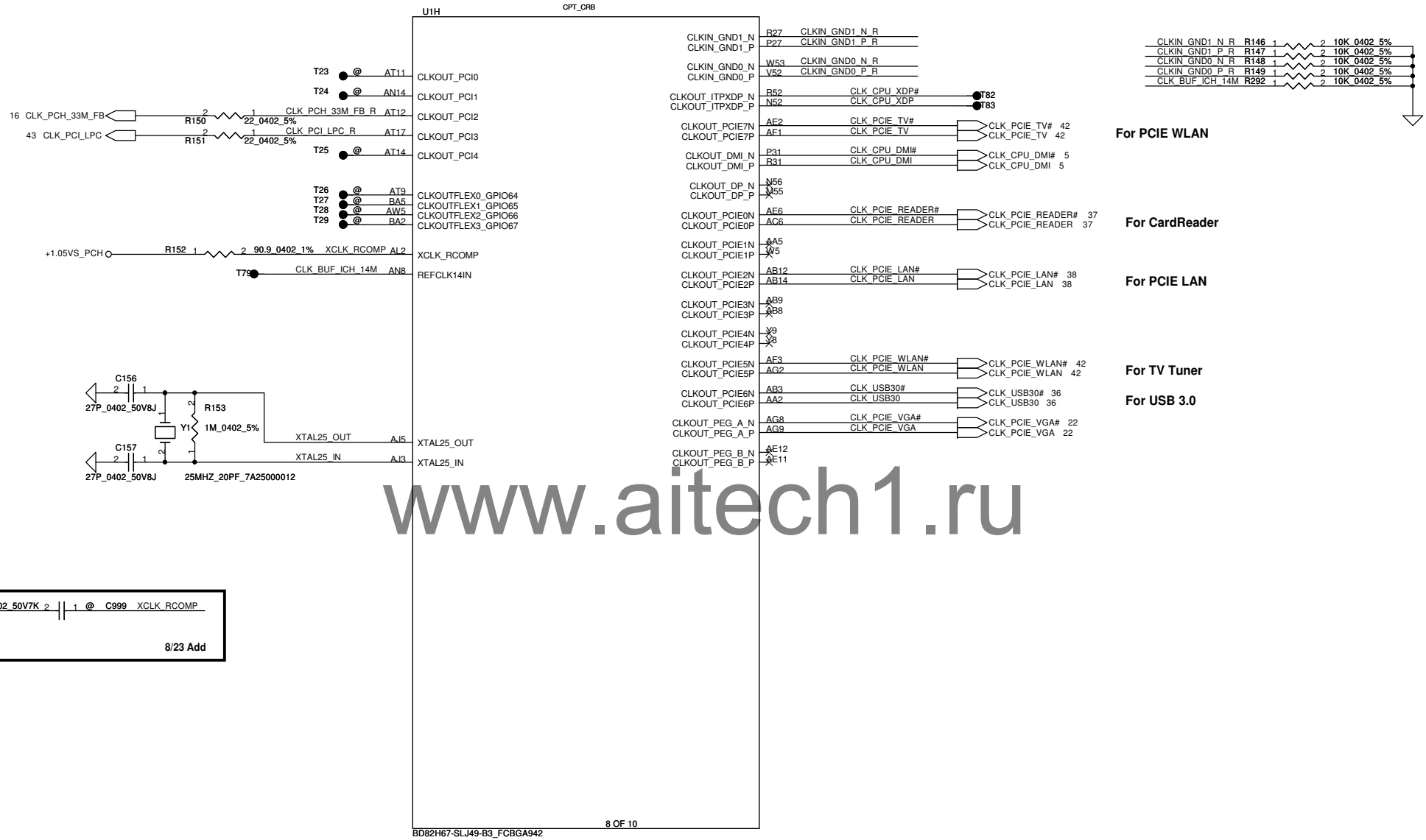
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PCH (5/9) PCI,FDI

Size: Custom | Document Number: QLA01 M/B LA-7811P Schematic | Rev: 1.A

Date: Thursday, June 16, 2011 | Sheet 16 of 63



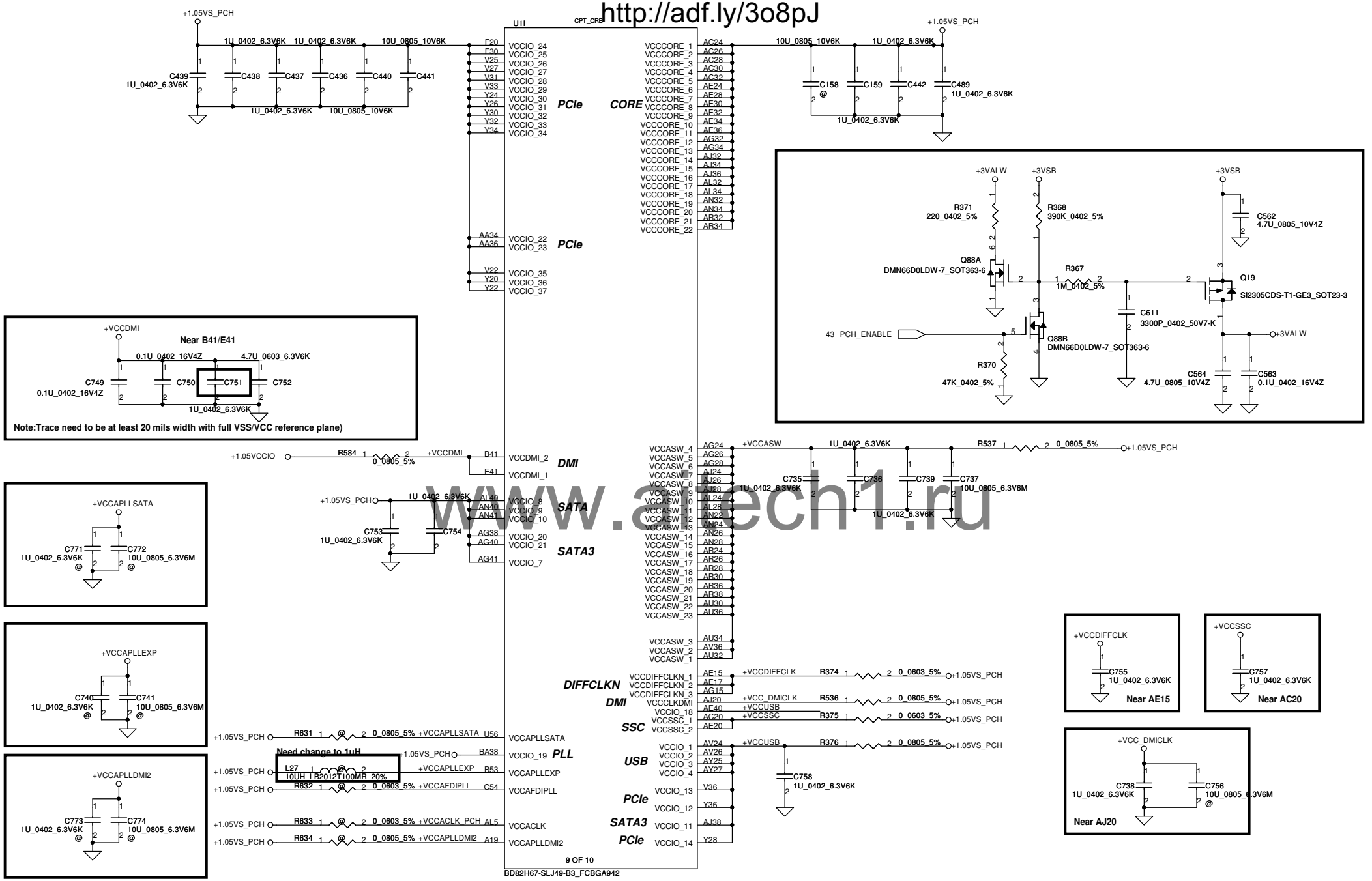
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PCH (6/9) CLOCK

Size: Custom | Document Number: QLA01 M/B LA-7811P Schematic | Rev: 1.A

Date: Thursday, June 16, 2011 | Sheet 17 of 63



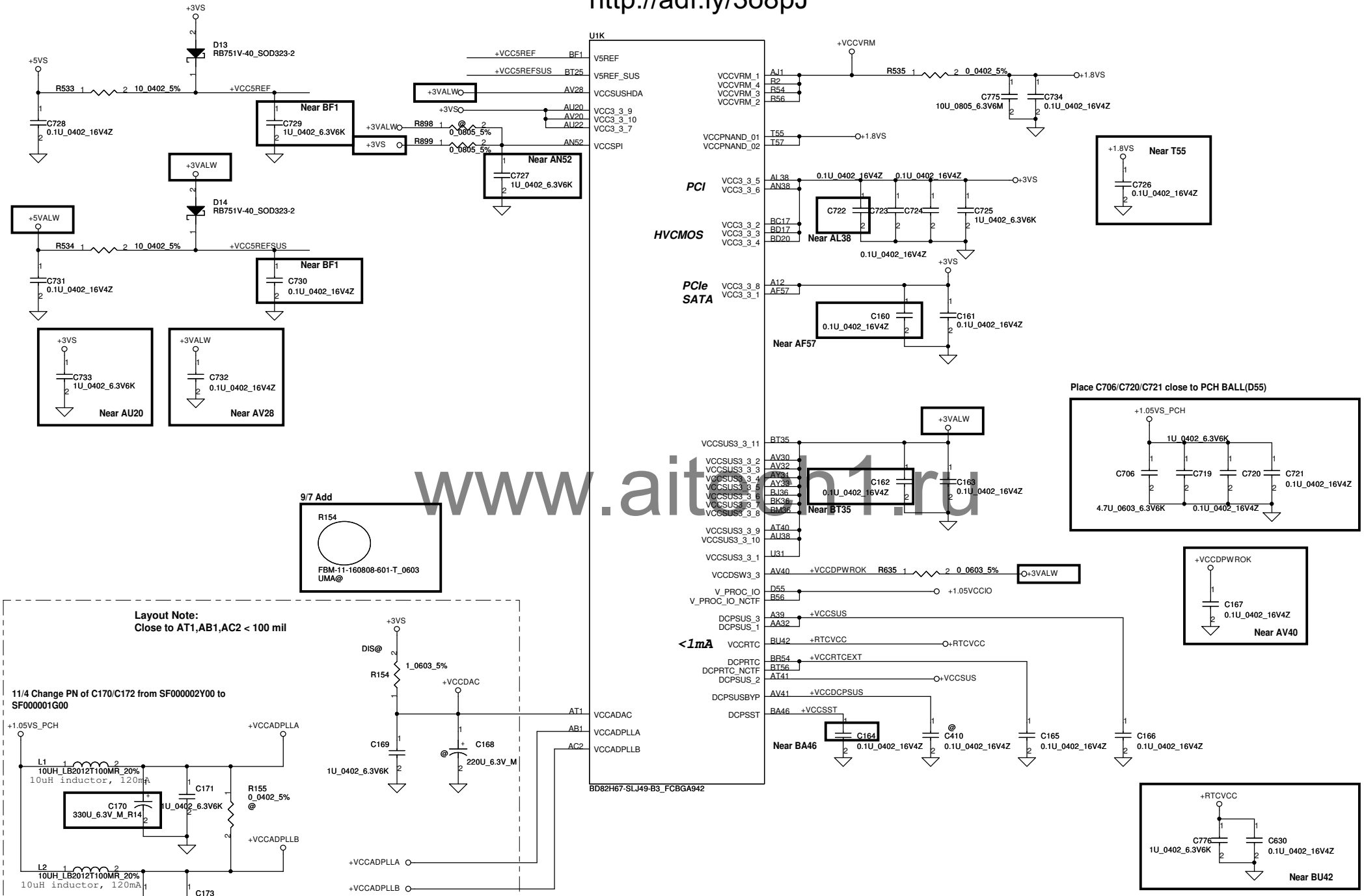
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: QLA01 M/B LA-7811P Schematic | Rev: 1.A

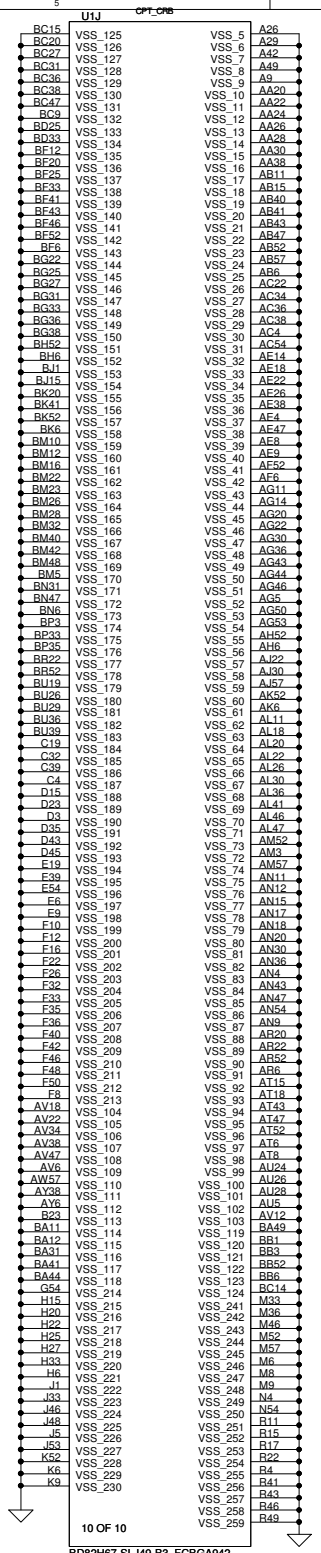
Date: Thursday, June 16, 2011 | Sheet 18 of 63

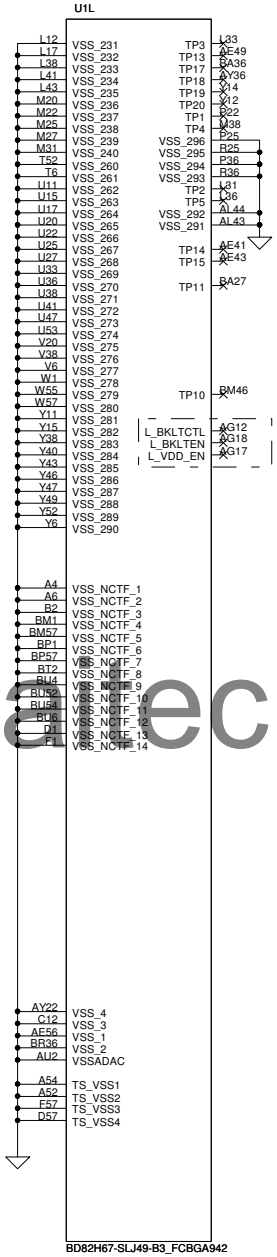


Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title	PCH (8/9) PWR	
Size: Custom	Document Number: QLA01 M/B LA-7811P Schematic	Rev: 1.A
Date: Thursday, June 16, 2011	Sheet 19 of 63	





NOTE:PCH adds support for panel power sequencing required for embedded DisplayPort support. L_VDDEN, L_BKLTEN and L_BKLTCTL pins are added on the PCH for panel power sequencing. It is important to note that a 6 layer board design may be required to access these pins on the PCH package in a fully featured platform design.

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

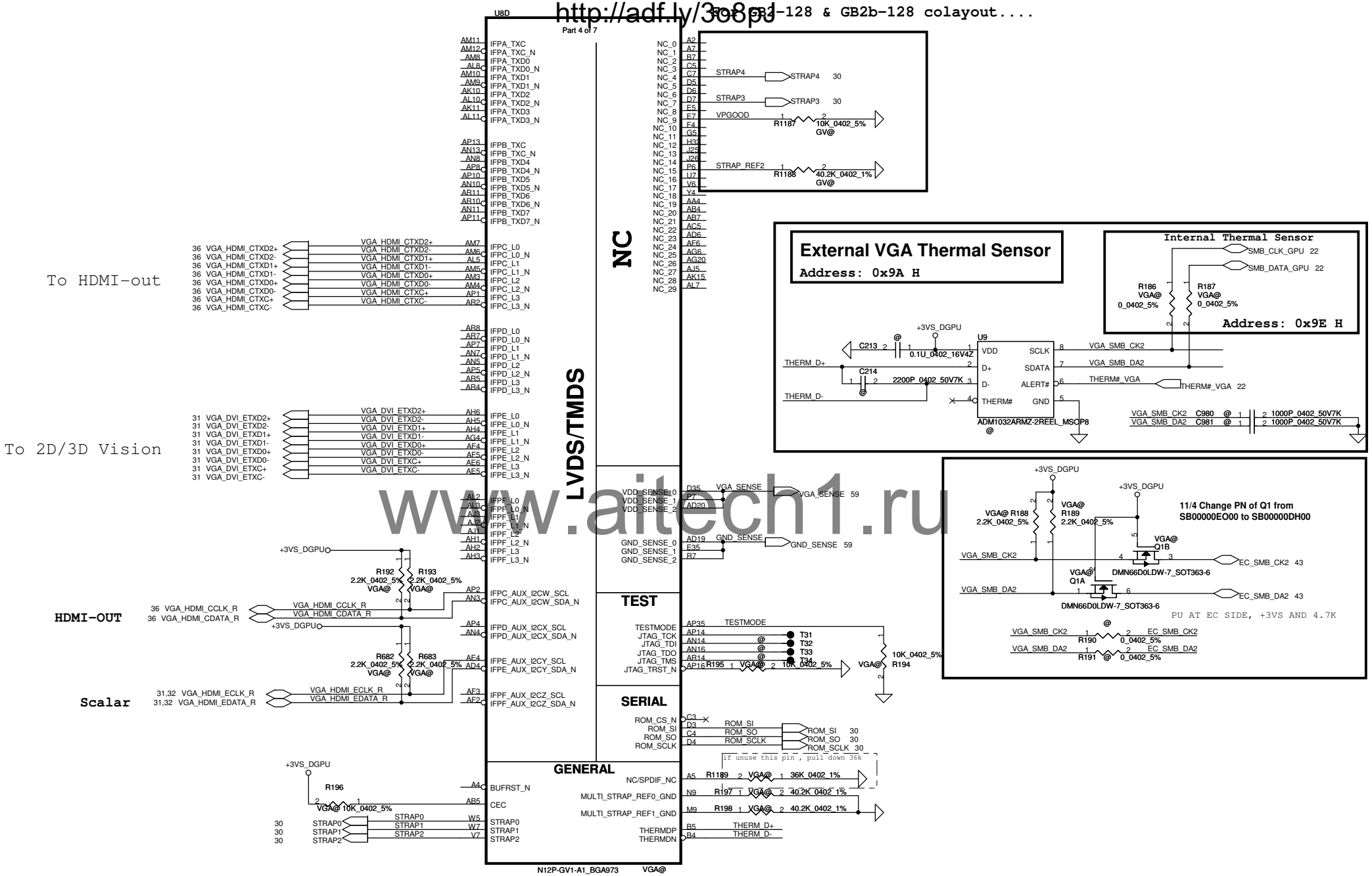
Compal Electronics, Inc.

Title: **PCH(9/9)VSS**

Size	Document Number	Rev
Custom	QLA01 M/B LA-7811P Schematic	1.A

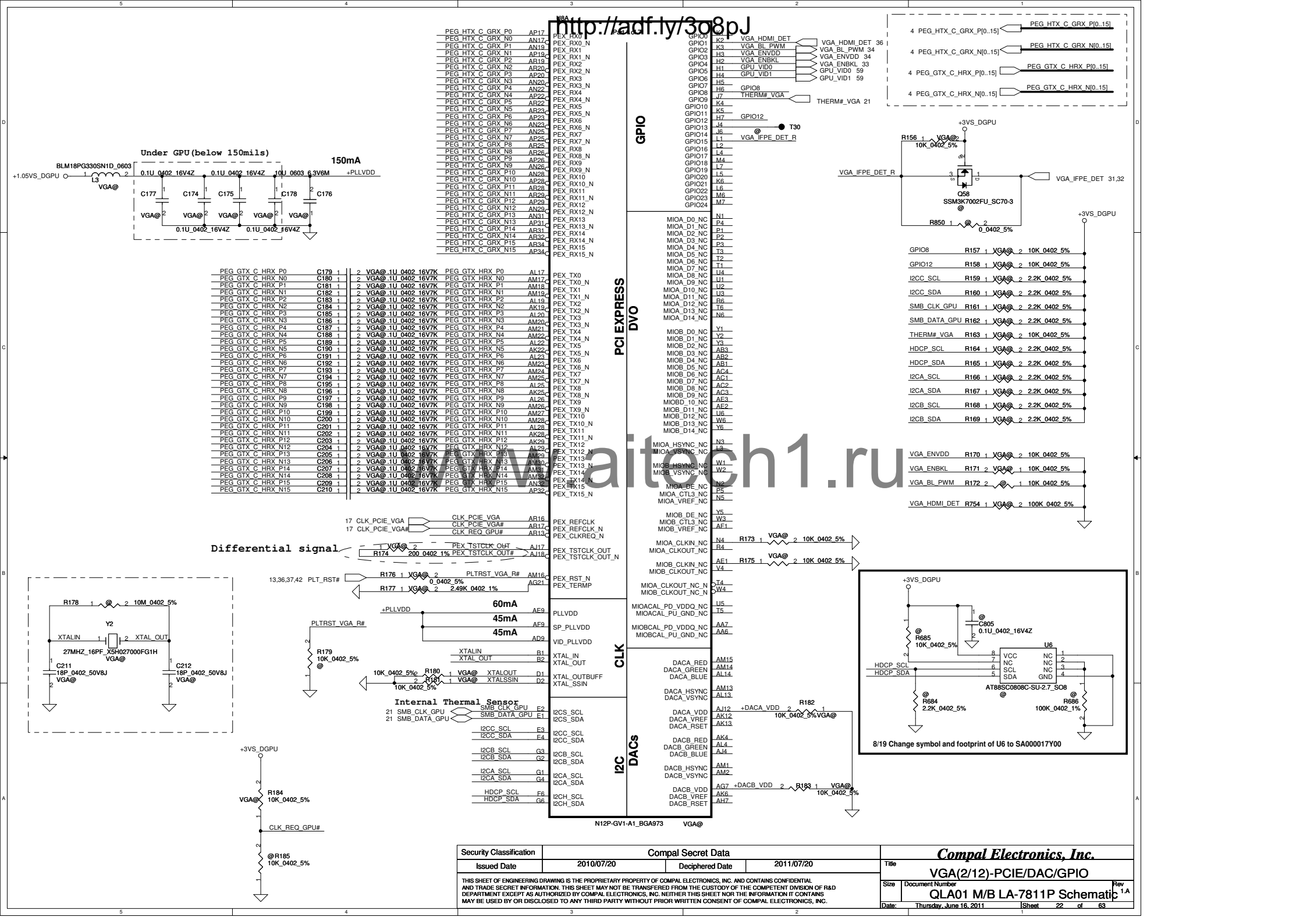
Date: Thursday, June 16, 2011 Sheet 20 of 63

GB2b-128 & GB2b-128 colayout....



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.	
Title	VGA(1/12)-LVDS/HDMI/DP/THM
Size	Document Number: QLA01 M/B LA-7811P Schematic
Rev	1.A
Date: Thursday, June 16, 2011	Sheet 21 of 63



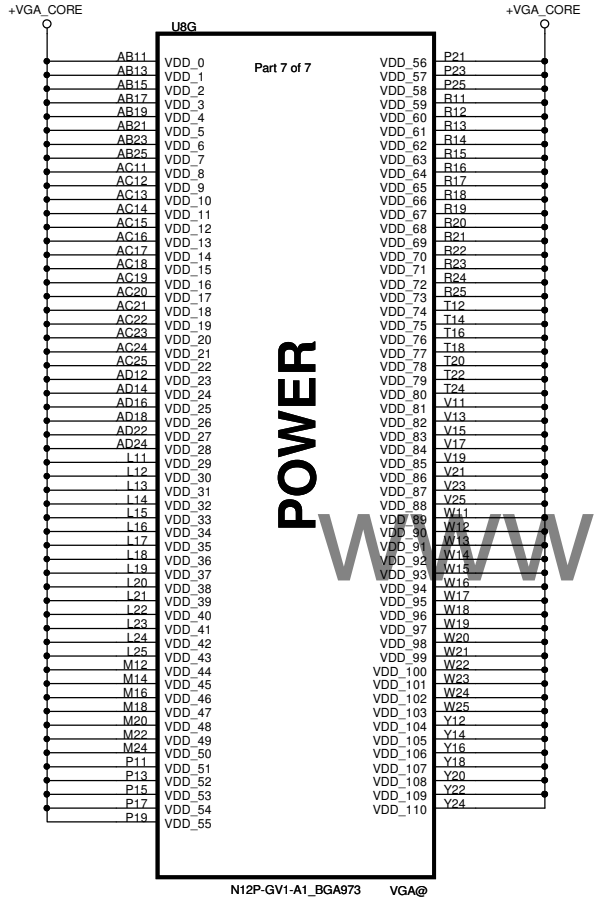
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

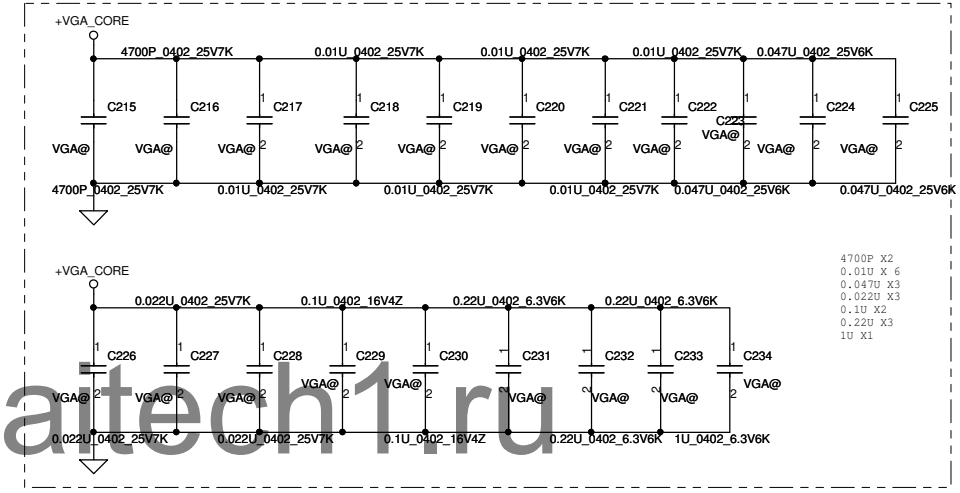
Title: VGA(2/12)-PCIE/DAC/GPIO

Size: | Document Number: QLA01 M/B LA-7811P Schematic | Rev: 1.A

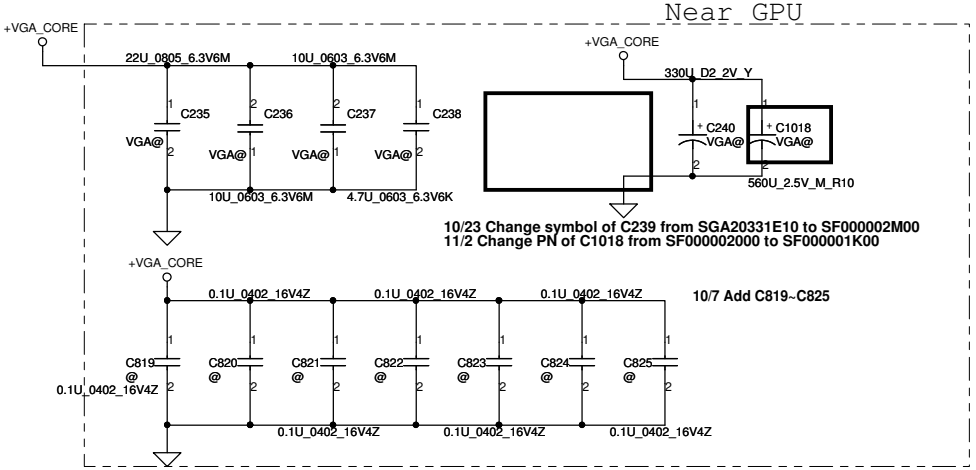
Date: Thursday, June 16, 2011 | Sheet 22 of 63



Under GPU



Near GPU



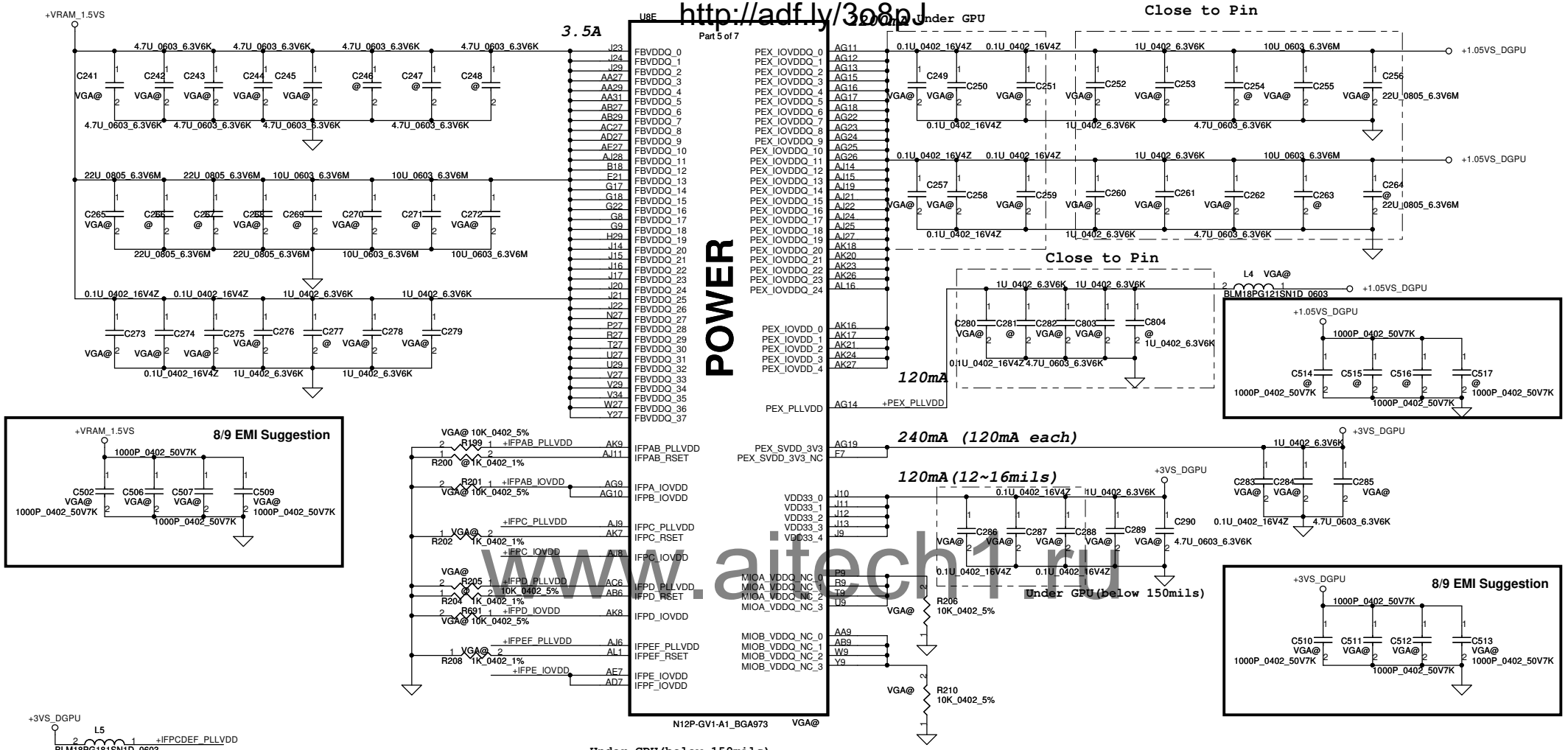
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: VGA(3/12)-VGA CORE

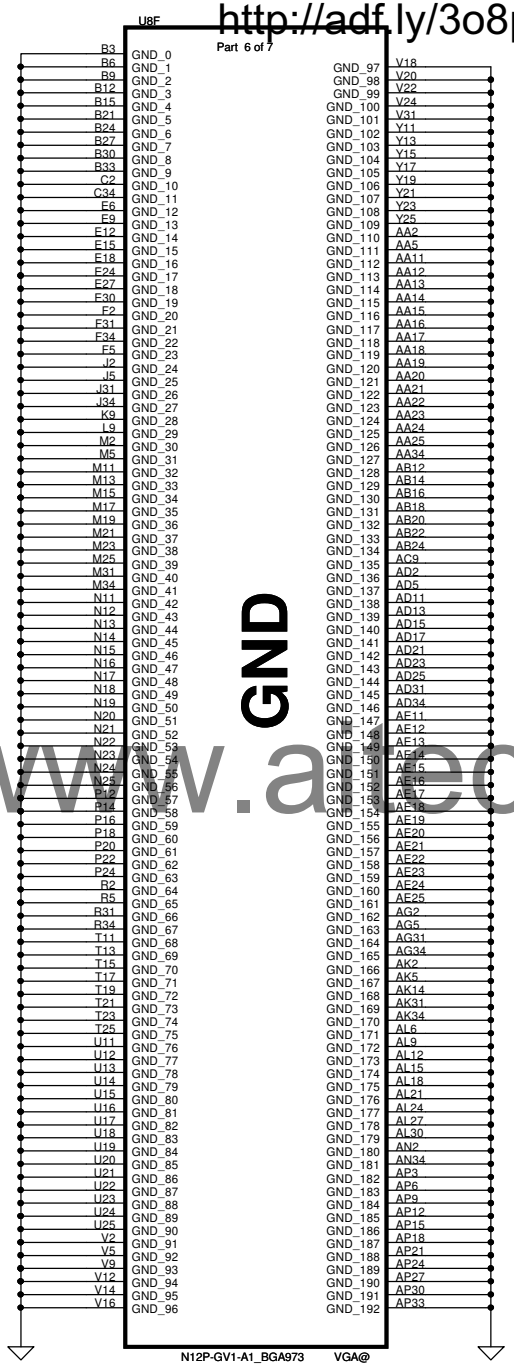
Size	Document Number	Rev
	QLA01 M/B LA-7811P Schematic	1.A

Date: Thursday, June 09, 2011 Sheet 23 of 63



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

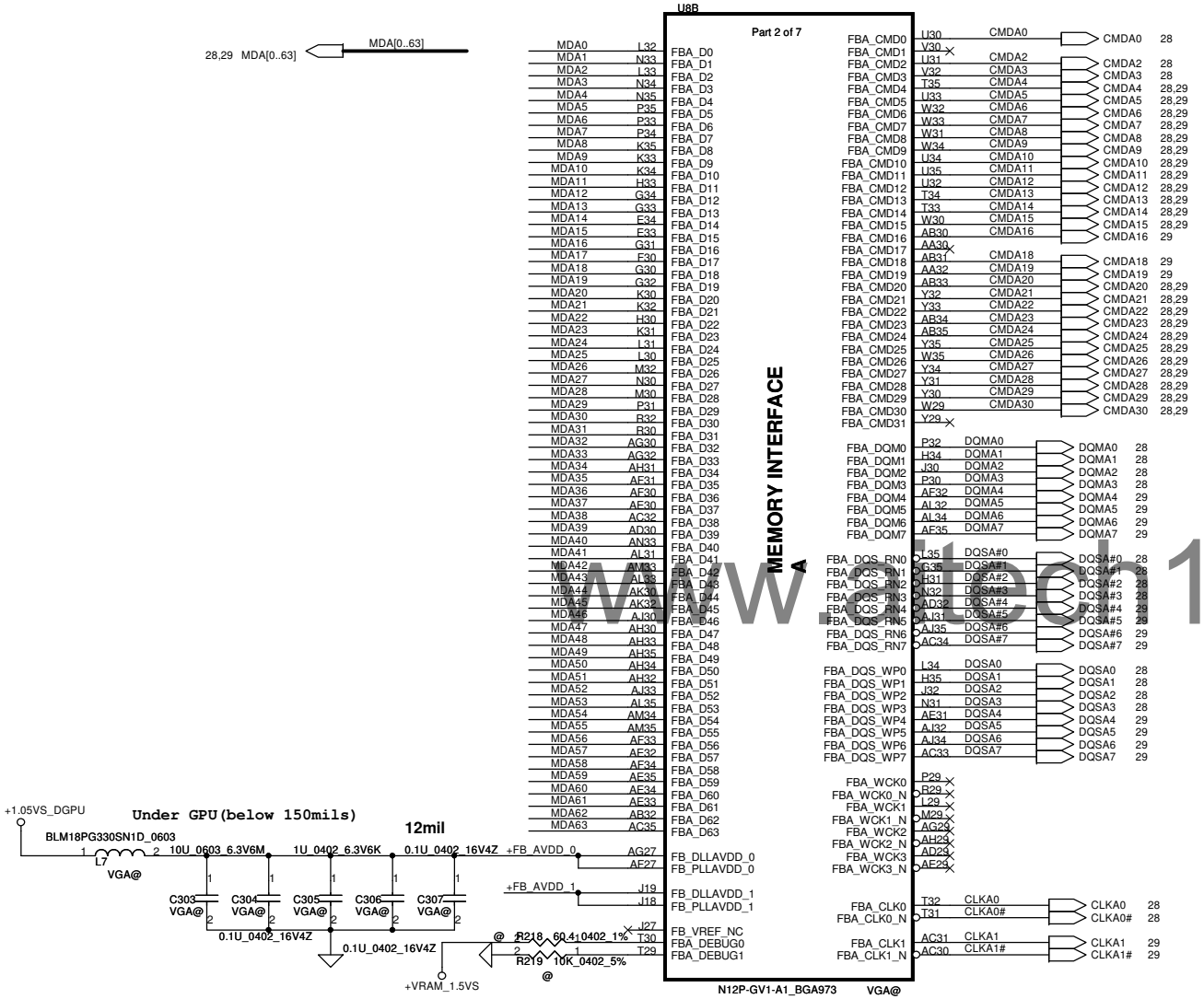
Compal Electronics, Inc.			
Title	VGA(4/12)-POWER		
Size	Document Number		Rev
	QLA01 M/B LA-7811P Schematic		1.A
Date:	Thursday, June 09, 2011	Sheet	24 of 63



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

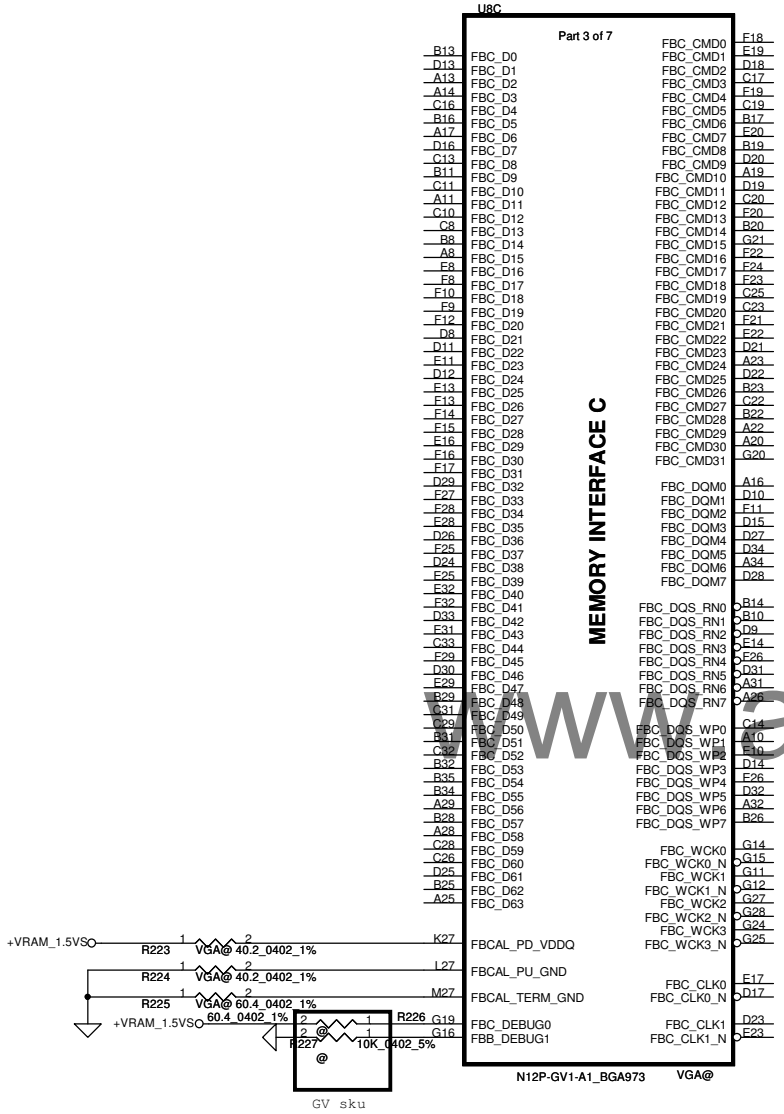
Title	VGA(5/12)-GND	
Size	Document Number	Rev
	QLA01 M/B LA-7811P Schematic	1.A
Date: Thursday, June 09, 2011	Sheet 25 of 63	



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title	VGA(6/12)-MEM Interface A
Size	Document Number: QLA01 M/B LA-7811P Schematic
Rev	1.A
Date:	Thursday, June 16, 2011
Sheet	26 of 63



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

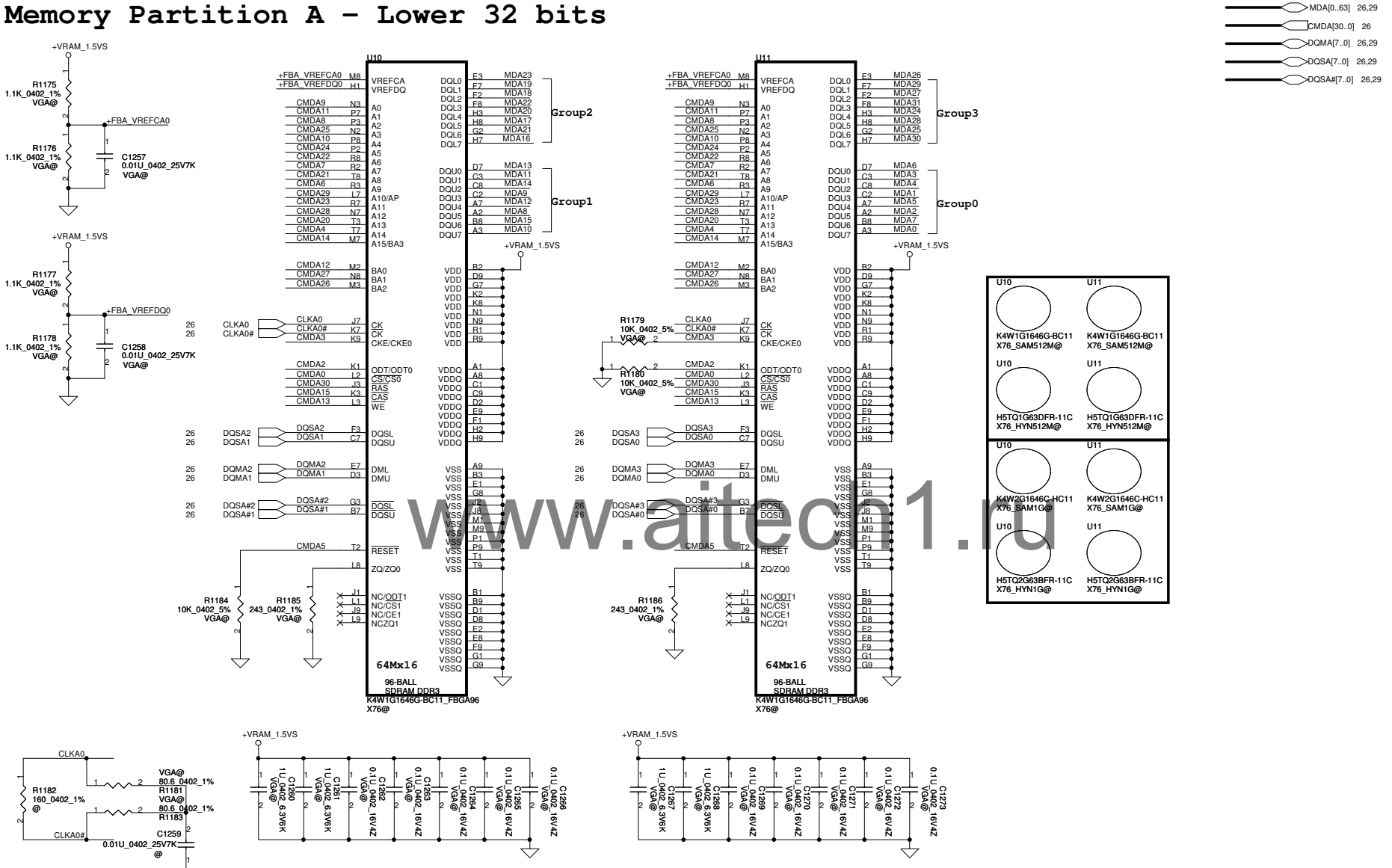
Compal Electronics, Inc.

Title: VGA(7/12)-MEM Interface C

Size | Document Number: QLA01 M/B LA-7811P Schematic | Rev: 1.A

Date: Thursday, June 09, 2011 | Sheet 27 of 63

Memory Partition A – Lower 32 bits



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

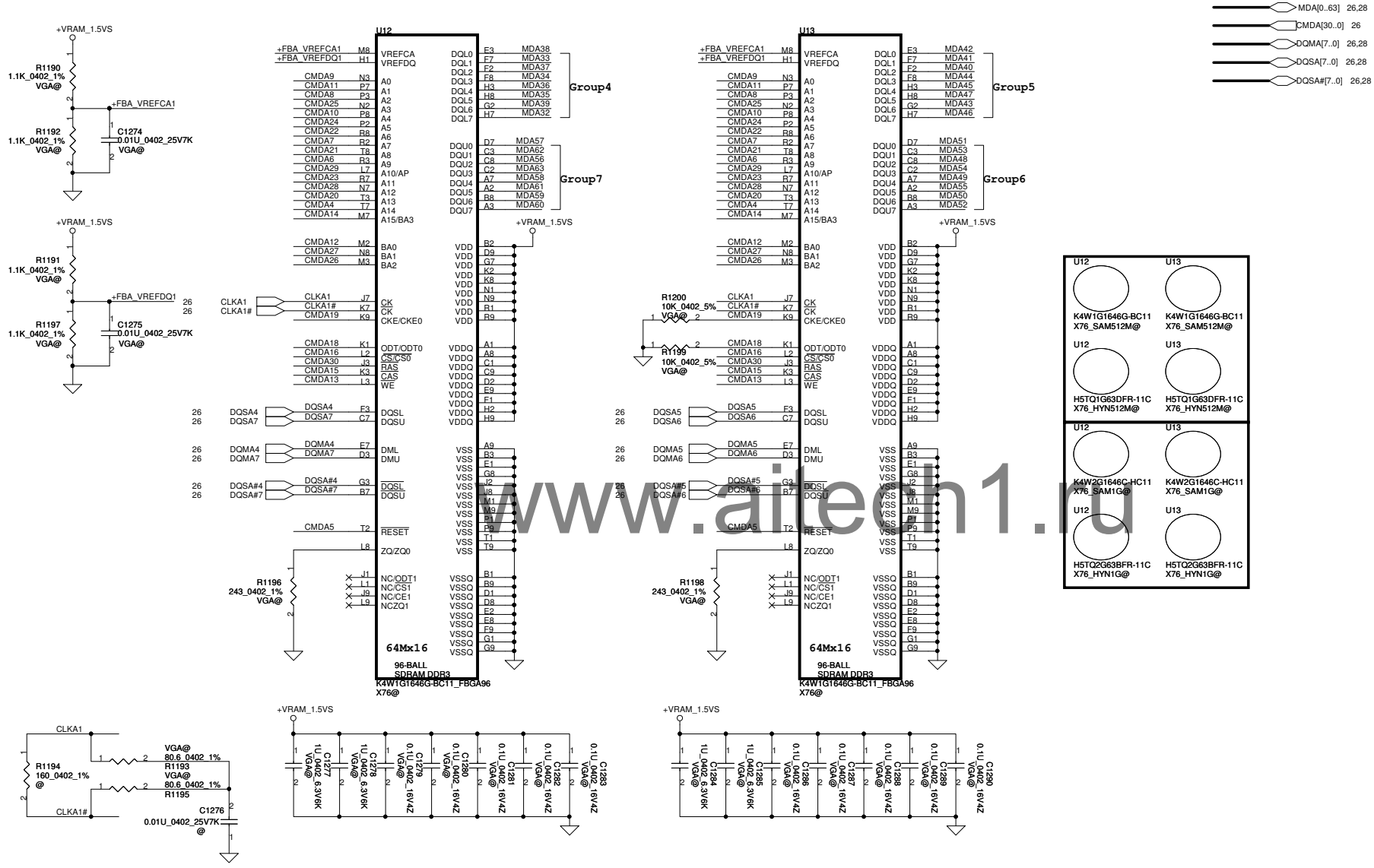
Compal Electronics, Inc.

Title: **VRAM_DDR3/ Channel A**

Size: Custom | Document Number: QLA01 M/B LA-7811P Schematic | Rev: 1.A

Date: Thursday, June 16, 2011 | Sheet 28 of 63

Memory Partition A – Upper 32 bits

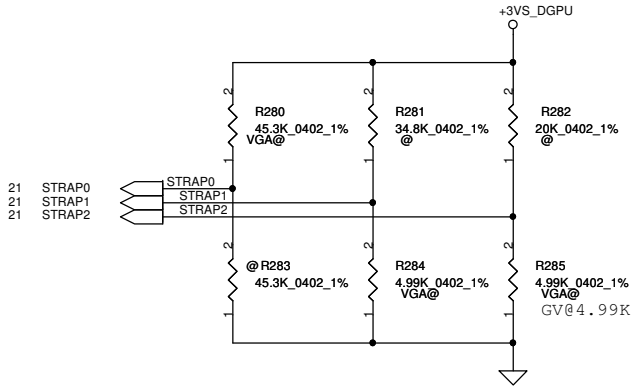


Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

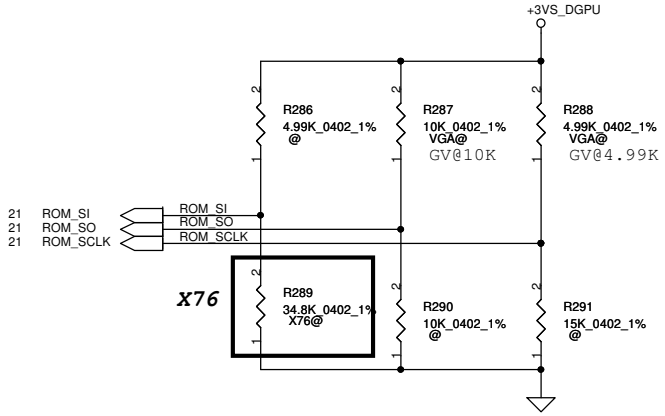
Title: **VRAM_DDDR5 / Channel A**

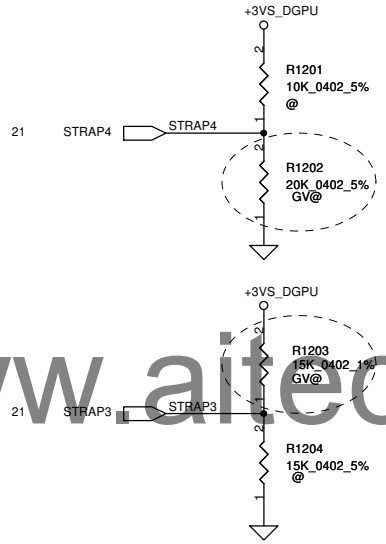
Size	Document Number	Rev
Custom	QLA01 M/B LA-7811P Schematic	1A
Date: Thursday, June 16, 2011	Sheet 29 of 63	

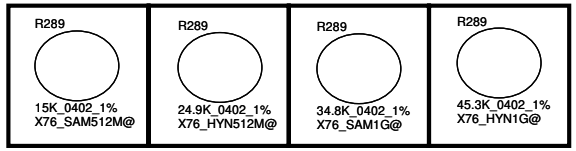


Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Physical Strapping pin		Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	GS	+3VGS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
	GV		FB[1]	FB[0]		
ROM_SCLK	GS	+3VGS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
	GV				PCI_DEVID[5]	
ROM_SI		+3VGS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP0		+3VGS	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1		+3VGS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2		+3VGS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3		+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4		+3VGS	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33V







GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N12P-GV	900 MHz	64M* 16* 4 512MB	K4W1G1646G-BC11 SA00004GS00	1111 R1221 PU 45K	0000 R1235 PD 5K	0000 R1226 PD 5K	1010 R1642 PU 15K	0011 R1644 PD 20K	0010 R289 PD 15K	1001 R1228 PU 10K	1000 R1229 PU 5K
N12P-GV	900 MHz	64M* 16* 4 512MB	H5TQ1G63DFR-11C SA000041S20	1111 R1221 PU 45K	0000 R1235 PD 5K	0000 R1226 PD 5K	1010 R1642 PU 15K	0011 R1644 PD 20K	0100 R289 PD 25K	1001 R1228 PU 10K	1000 R1229 PU 5K
N12P-GV	900 MHz	128M* 16* 4 1GB	K4W2G1646C-HC11 SA000047Q00	1111 R1221 PU 45K	0000 R1235 PD 5K	0000 R1226 PD 5K	1010 R1642 PU 15K	0011 R1644 PD 20K	0110 R289 PD 35K	1001 R1228 PU 10K	1000 R1229 PU 5K
N12P-GV	900 MHz	128M* 16* 4 1GB	H5TQ2G63BFR-11C SA00003YO30	1111 R1221 PU 45K	0000 R1235 PD 5K	0000 R1226 PD 5K	1010 R1642 PU 15K	0011 R1644 PD 20K	0111 R289 PD 45K	1001 R1228 PU 10K	1000 R1229 PU 5K

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

User [3:0]	
1111	EDID is used 1920x1080
1000-1100	Customer defined

3GIO_PADCFG[3:0]	
0000	RESERVED
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLOCK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

PCIE_MAX_SPEED	
1	Default

DP_PLL_VDD33V	
0	Default

GPU	Package	DeviceID	PCI_DEVID[5..0]
N12P-GS	GB2-128	0x0DF4	(..1111 0100)
N12P-GV-B	GB2b-128	0x1050	(..0101 0000)

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: VGA(12/12)-MISC

Size: Custom | Document Number: QLA01 M/B LA-7811P Schematic | Rev: 1.A

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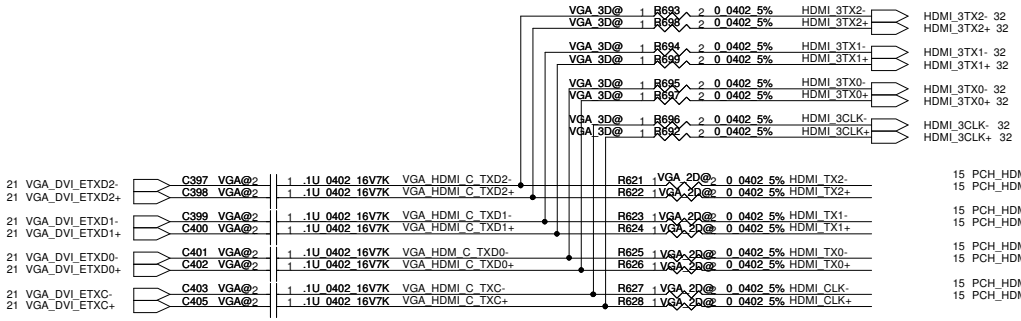
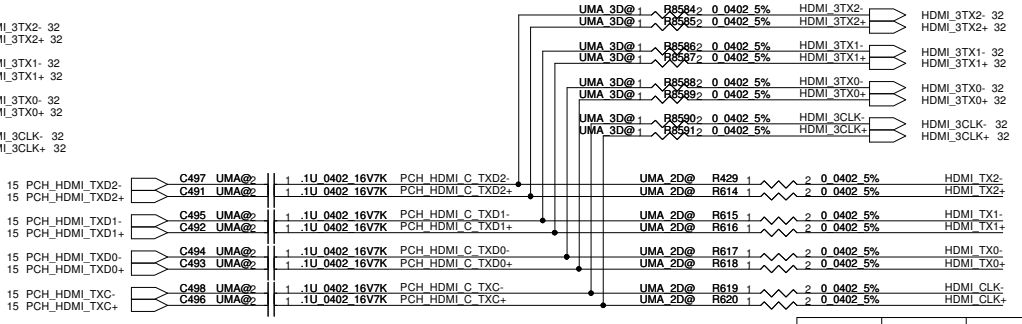
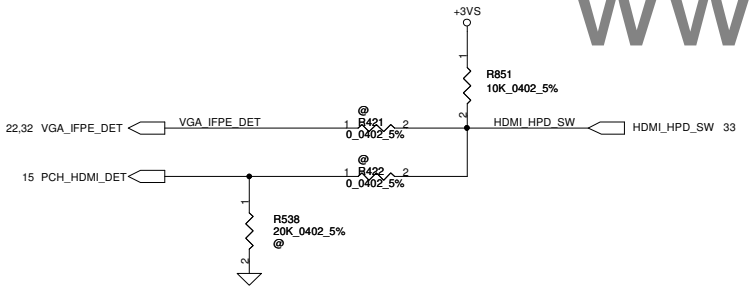
0804 Vendor suggest close to Cap.

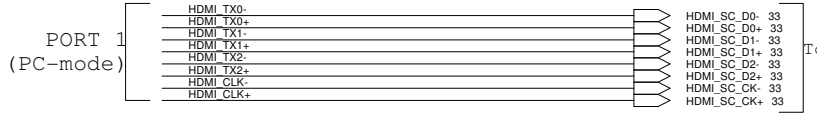


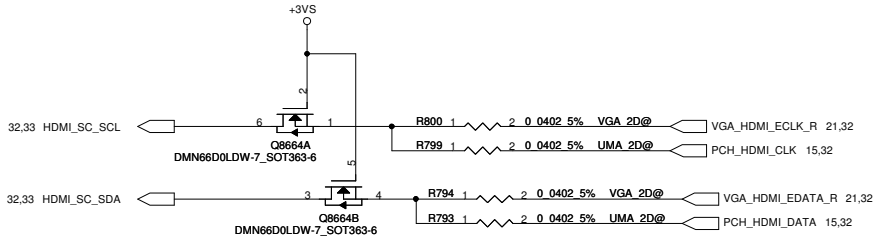
0804 Vendor suggest close to Cap.



S2 (pin33)	S1 (pin32)	TMDS/DDC output
H	H	PORT1/SCL1,SDA1
H	L	PORT2/SCL2,SDA2
L	H	All disconnected







Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

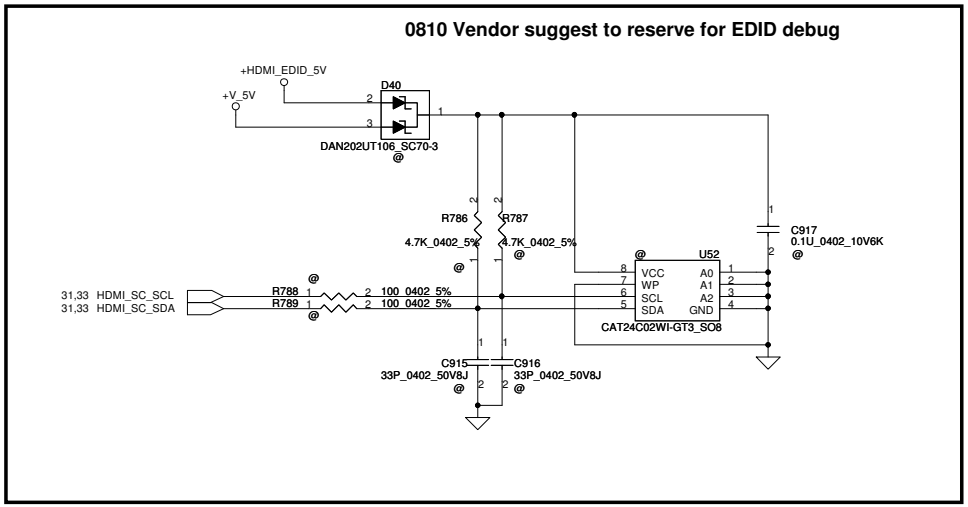
Compal Electronics, Inc.

Title: HDMI Switch

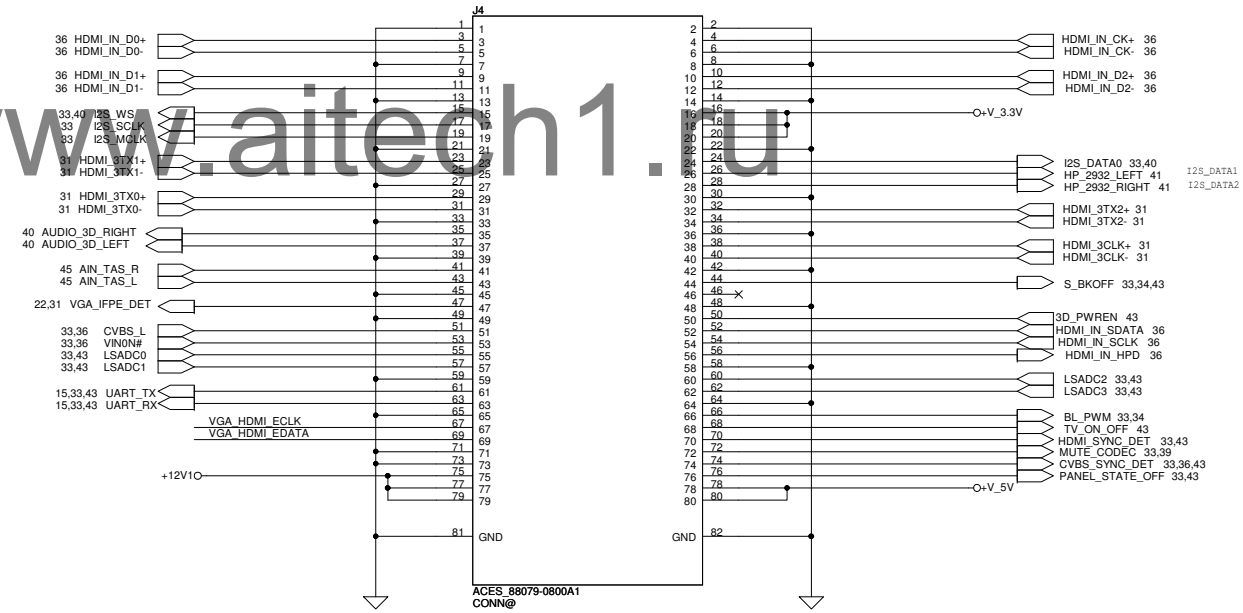
Size: Custom | Document Number: QLA01 M/B LA-7811P Schematic | Rev: 1.A

Date: Thursday, June 16, 2011 | Sheet 31 of 63

0810 Vendor suggest to reserve for EDID debug



12/11 3D Scaler Pin define update



12/6 Change symbol of J4 from LTCX002TM00 to SP010011B00(60pin to 80pin)

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: 3D Scalar

Size: Custom | Document Number: QLA01 M/B LA-7811P Schematic | Rev: 1.A

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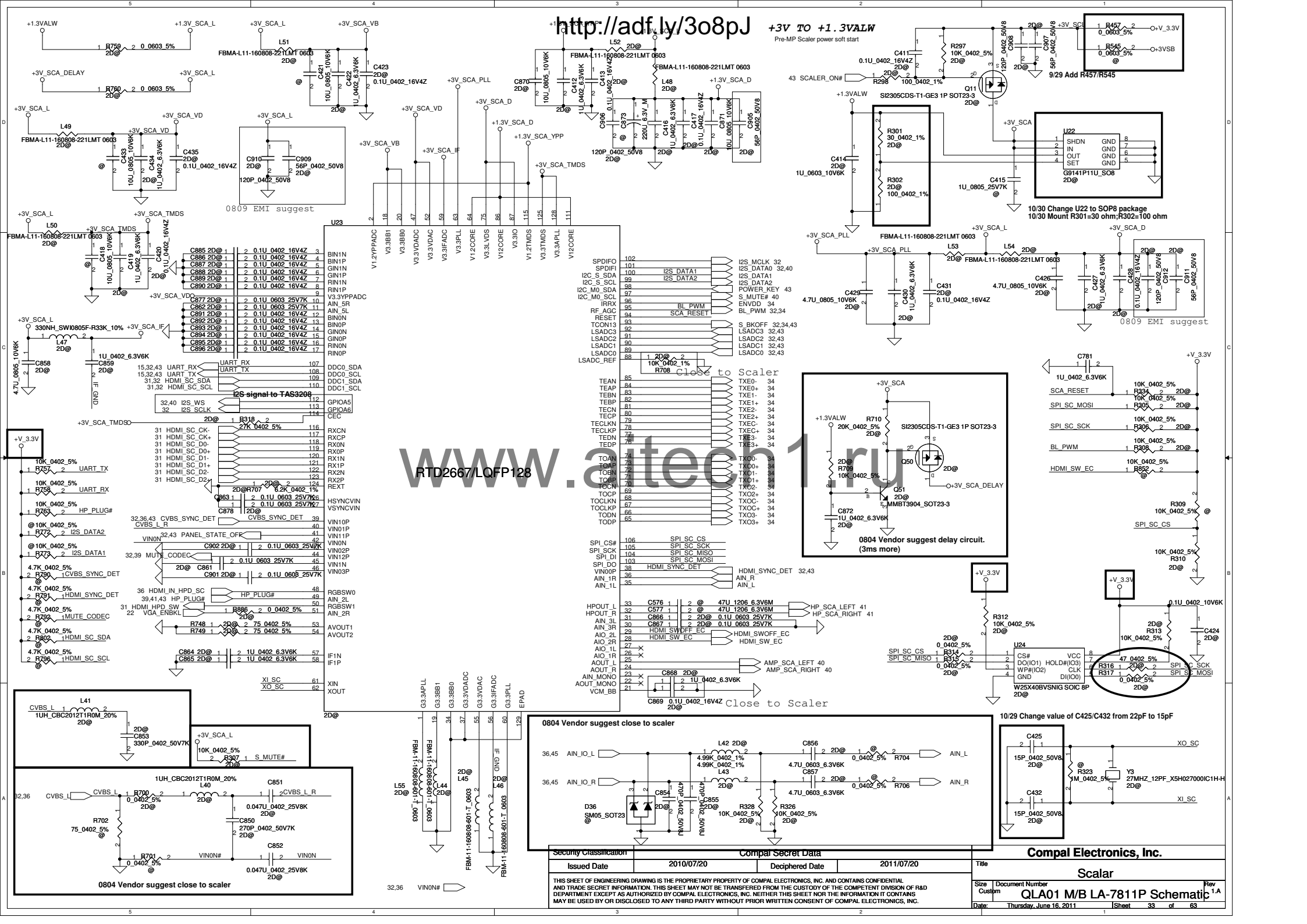

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: Scalar

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WebCam+Digital Mic

5/18 Change R332 from 100K to 10K ohm

135mA

+3VS

R331 1 2 0_0402_5%

40 mils

R332 @ 10K_0402_5%

C443 0.1U_0402_16V4Z

@ Q12 AO3413_SOT23-3

CAM_PWR

C444 10U_0603_6.3V6M

12 CAM_OFF — R335 @ 0_0402_5%

43 EC_CAM_OFF — R942 @ 0_0402_5%

14 USB20_P5 — USB20_P5 — R330 WCM-2012-900T_0805 0_0402_5% — USB20_P5_R

14 USB20_N5 — USB20_N5 — L15 @ — USB20_N5_R

CAM_PWR

R333 0_0402_5%

39 DMIC_DATA — L68 FBMA-10-100505-301T_2P — DMIC_DATA_R

39 DMIC_CLK — L69 FBMA-10-100505-301T_2P — DMIC_CLK_R

R965 0_0402_5%

INT_MIC

JCAM1 — ACES_87213-0800N CONN@

11/30 Del R969/R970

11/30 Add L68/L69=SM01000CY00

11/28 Change symbol of JCAM1 from SP02000RQ00 to SP02000S300

10/27 Add D49(ESD request)

D49 — DMIC_DATA_R — DMIC_CLK_R — PESD5V0U2BT_SOT23-3 <ESD>

+3VS

R437 10K_0402_5% @

MIC_INT_VREFO — R797 0_0402_5% — R810 2.2K_0402_5% — INT_MIC

R703 1K_0402_5% — INT_MIC_RIGHT 39

C453 0.1U_0402_16V4Z @

R809 27K_0402_5% @

R742 0_0402_5%

D41 — PESD5V0U2BT_SOT23-3 <EMI>

R705 1K_0402_5% — INT_MIC_LEFT 39

LVDS CONN

JLVDS1 — ACES_87242-3001-09 CONN@

33 TXO0+ — TXO0- 33

33 TXO1+ — TXO1- 33

33 TXO2+ — TXO2- 33

33 TXOC- — TXOC+ 33

33 TXO3- — TXO3+ 33

33 TXE0- — TXE0+ 33

33 TXE1+ — TXE1- 33

33 TXE2- — TXE2+ 33

33 TXEC- — TXEC+ 33

33 TXE3- — TXE3+ 33

+LCDVDD

C451 0.1U_0402_16V4Z 2D@

C452 0.1U_0402_16V4Z 2D@

C448 2D@ 680P_0402_50V7K

+LCDVDD

LVDS POWER

+LCDVDD — R336 220_0402_5% 2D@

+5VSB — R337 390K_0402_5% 2D@

Q13A DMN66D0LDW-7_SOT363-6 2D@

R339 1M_0402_5% 2D@

11/4 Change PN of Q13 from SB570025280 to SB00000DH00

22 VGA_ENVDD — R419 0_0402_5%

33 ENVDD — R420 0_0402_5%

43 EC_ENVDD — R881 0_0402_5%

Q13B DMN66D0LDW-7_SOT363-6 2D@

R341 47K_0402_5%

+V_5V — 1150mA

C446 4.7U_0805_10V4Z 2D@

120mil

Q14 SI2305CDS-T1-GE3_SOT23-3 2D@

C447 3300P_0402_50V7-K 2D@

120mil — 1150mA — +LCDVDD

C449 4.7U_0805_10V4Z 2D@

C450 0.1U_0402_16V4Z 2D@

INVERTER

ENVDD: scalar->EC-> inverter

INVT_PWM: scalar-> inverter

BKOFF#: scalar->EC-> inverter 10/20

950mA

+12V2 — L17 FBMA-L11-201209-221LMA30T_0805 — INVPWR_B+

C456 680P_0402_50V7K

C457 680P_0402_50V7K

22 VGA_BL_PWM — 0_0402_5% — R747

43 INVT_PWM — 0_0402_5% — R352

0_0402_5% — R351 — BL_PWM_R

32,33 BL_PWM

32,33,43 S_BKOFF — 0_0402_5% — R353 — S_BKOFF_R

43 BKOFF# — 0_0402_5% — R598

R354 4.7K_0402_5%

C499 680P_0402_50V7K

INVPWR_B+ — JINV1 — ACES_87213-1200G CONN@

Touch Panel

PVT change from alw to vs for EUP.

@D11 — PRTR5V0U2X_SOT143-4

+5VS — USB20_P4_R — USB20_N4_R

100mA

C458 0.1U_0402_16V4Z

@ C459 1U_0603_10V6K

14 USB20_N4 — USB20_N4 — 0_0402_5% — R345 — USB20_N4_R

14 USB20_P4 — USB20_P4 — 0_0402_5% — R346 — USB20_P4_R

JTOUCH — ACES_87213-0500G_5P CONN@

Shield GND

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.	
Title	LCD CONN. / WebCam
Size: Custom	Document Number: QLA01 M/B LA-7811P Schematic
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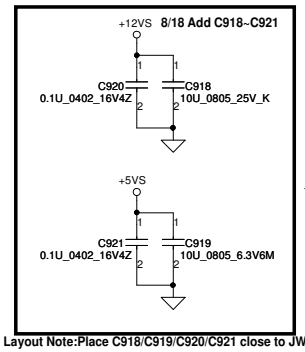
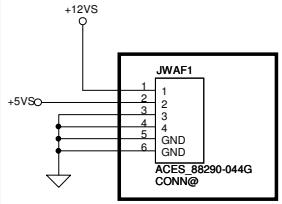
HDD POWER Conn



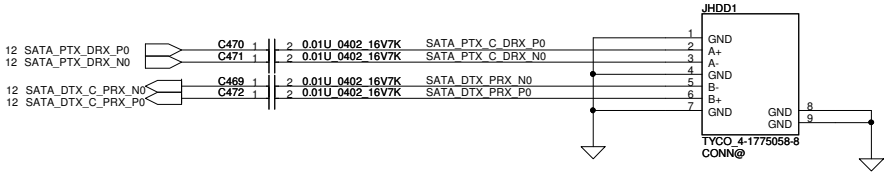
Layout Note:Place C918/C919/C920/C921 close to JWAFER1

HDD

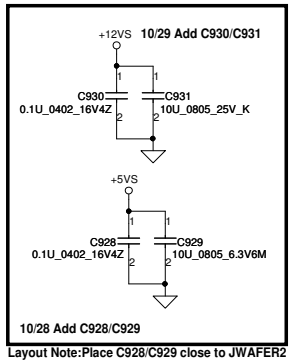


12/6 Change footprint of JWAF1 from SP02000AO00 to SP02000EB00

SATA HDD Conn.

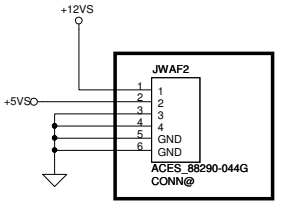


ODD POWER Conn



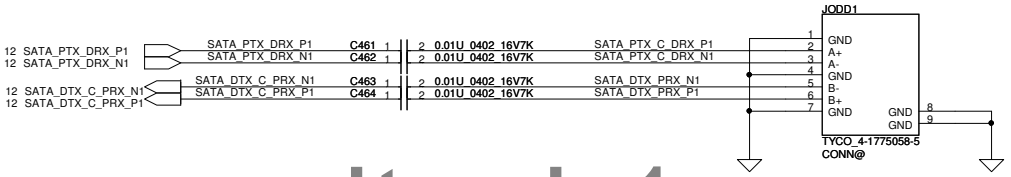
Layout Note:Place C928/C929 close to JWAFER2

ODD



12/6 Change footprint of JWAF1 from SP02000AO00 to SP02000EB00

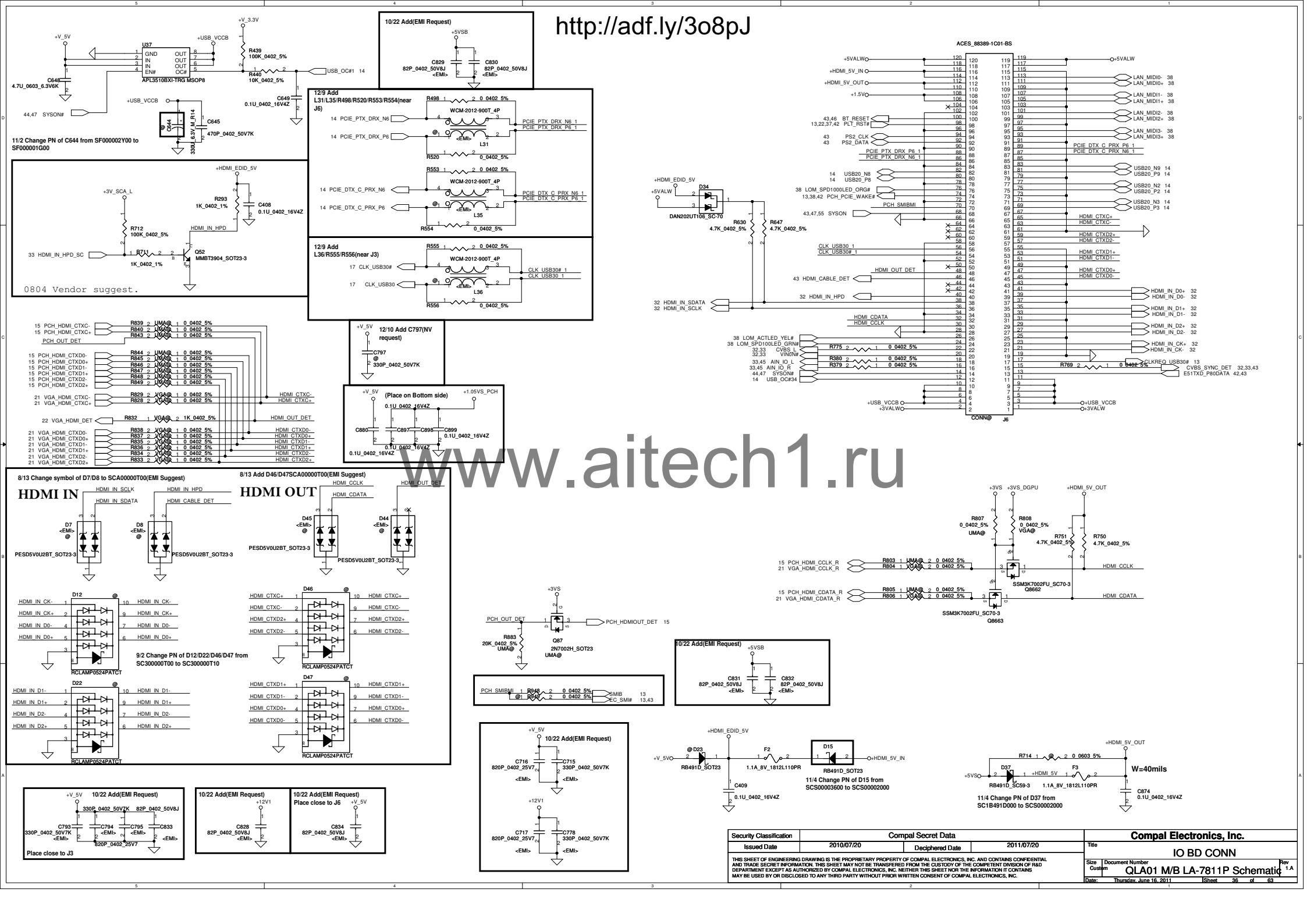
SATA ODD Conn.



SSD

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.	
Title	HDD & ODD & SSD Connector
Size B	Document Number QLA01 M/B LA-7811P Schematic Rev 1.A
Date: Thursday, June 16, 2011	Sheet 35 of 63



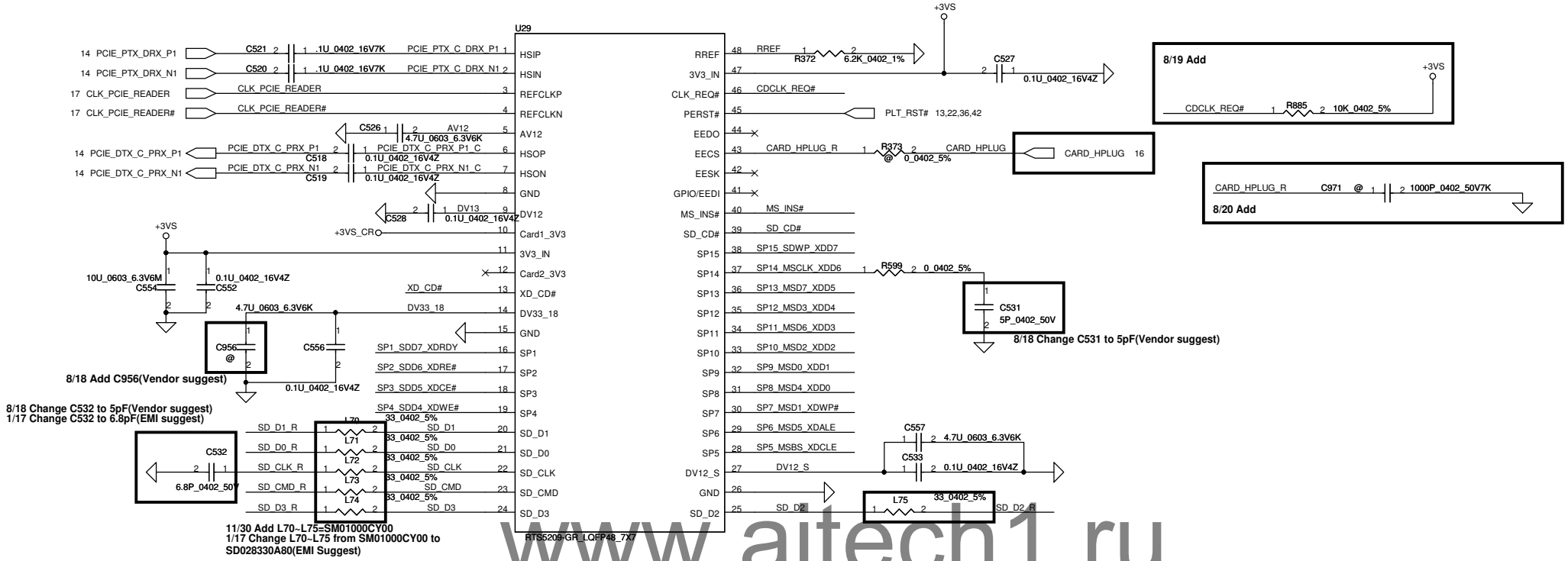
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

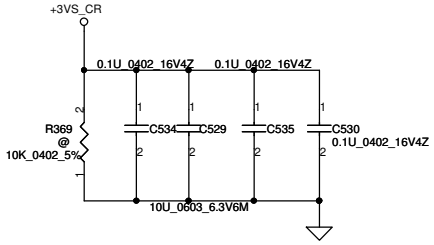
Compal Electronics, Inc.

Title: IO BD CONN

Size: Custom | Document Number: QLA01 M/B LA-7811P Schematic | Rev: 1.A

Date: Thursday, June 16, 2011 | Sheet 36 of 63





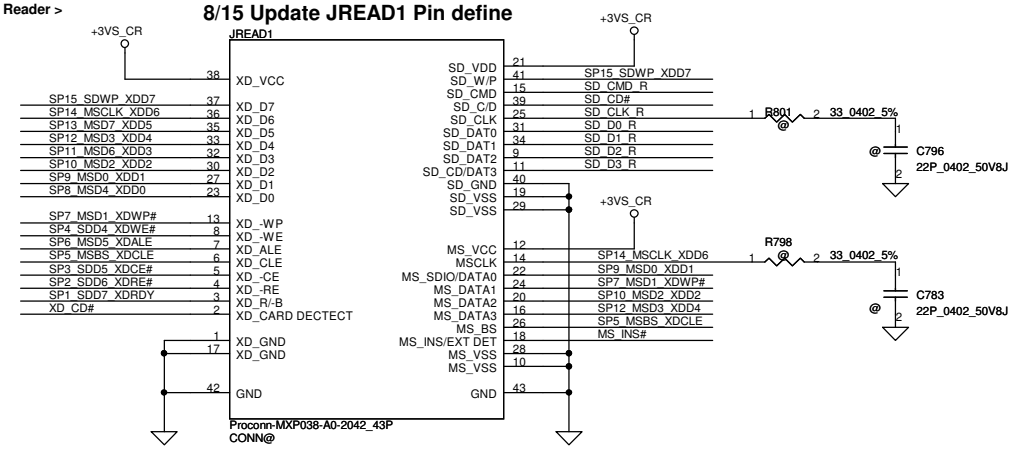
Place C534 close to socket pin 38

Place C529 close to socket pin 21

Place C535 close to socket pin 21

Place C530 close to socket pin 12

< 7 in 1 Card Reader >



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.			
Title	PCIE-Card Reader-RTS5209		
Size	Document Number		Rev
	QLA01 M/B LA-7811P Schematic		1.A
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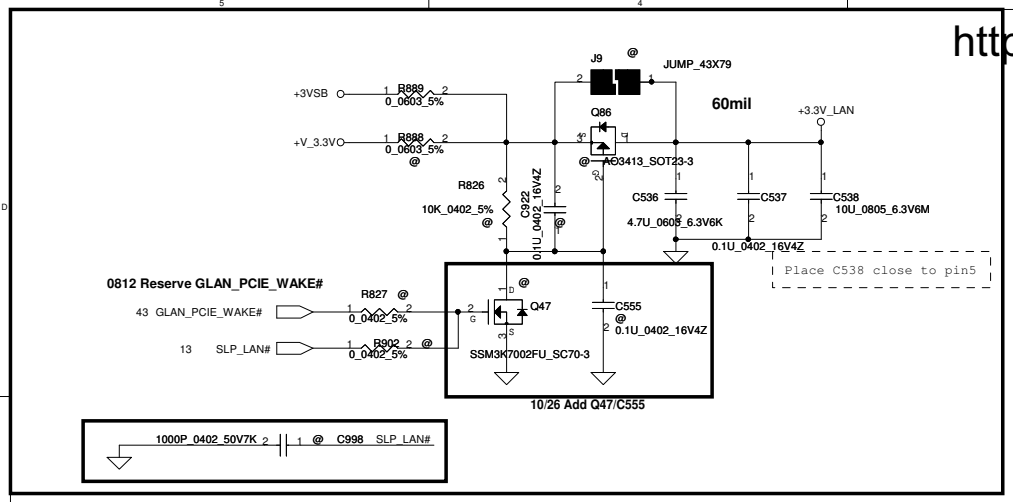
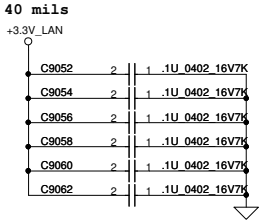
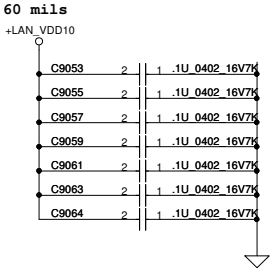


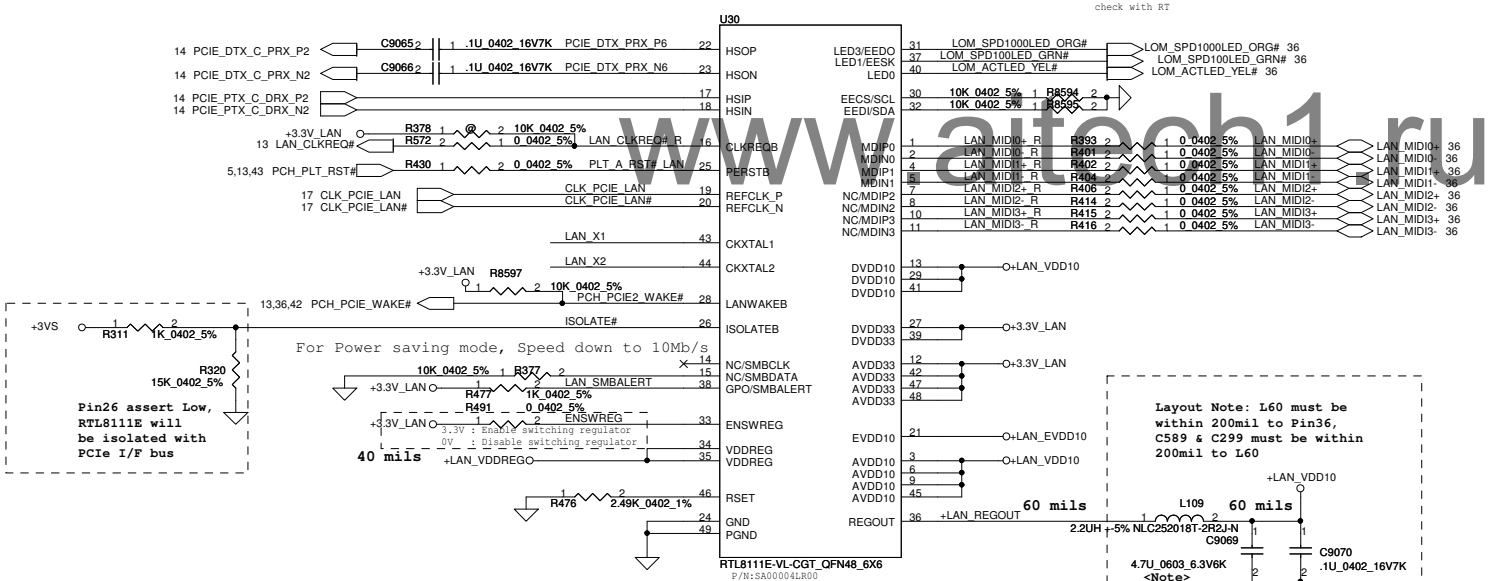
Power (Decoupling Cap.)

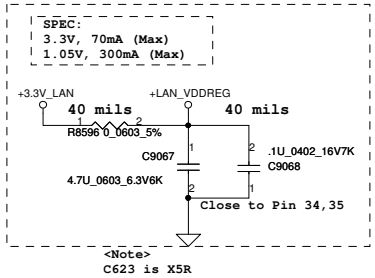


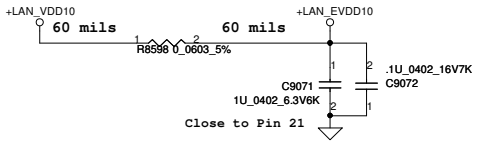
C625, C610, C617, C626 ,C621 , C604 close to Pin 12,27,39,42,47,48 , respectively



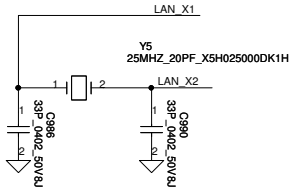
C615, C614,C622 ,C620, C616,C611,C624 close to pin 3,6,9,13,29,41,45, respectively







Crystal



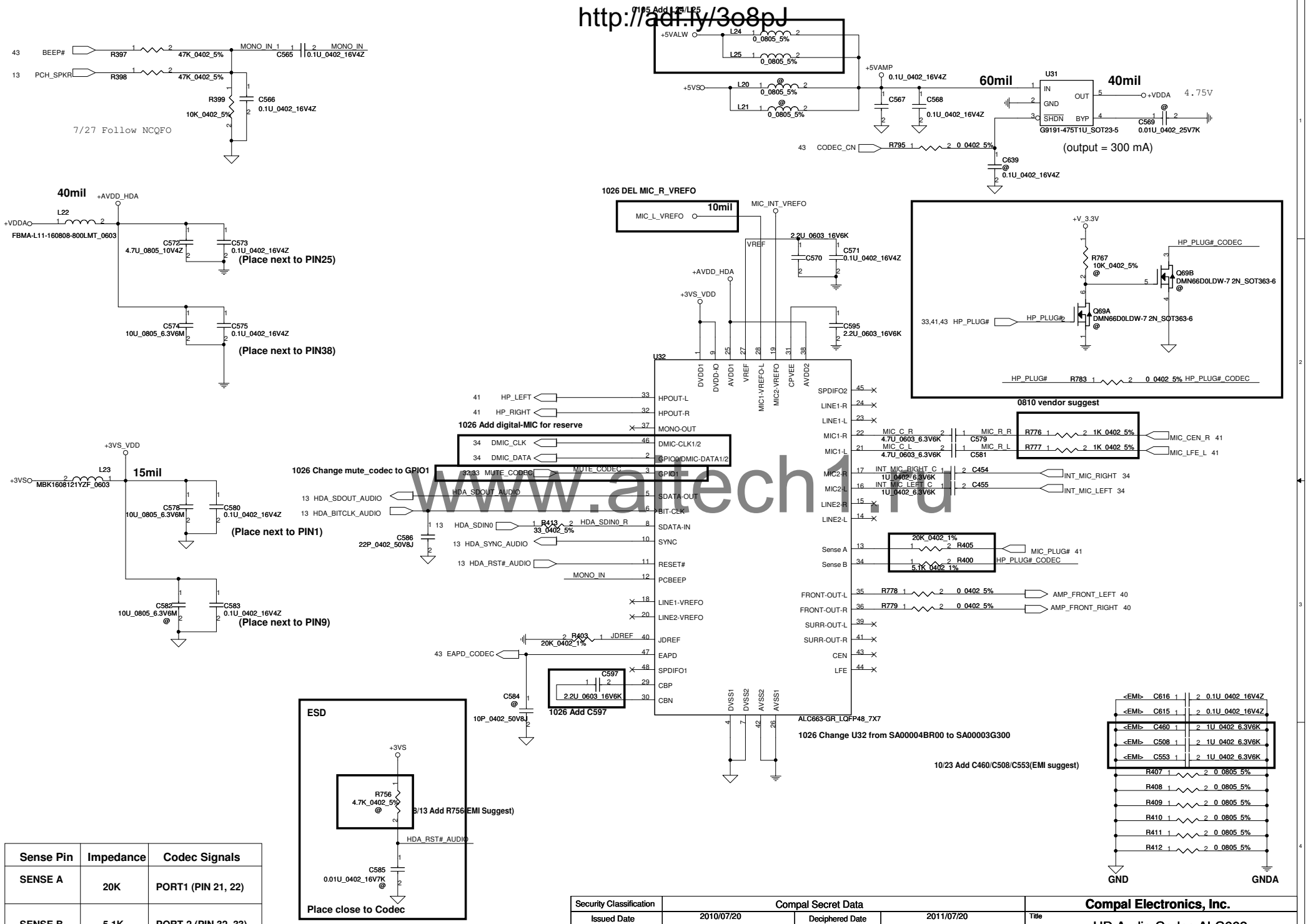
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: Intel LAN-82579

Size: Custom | Document Number: QLA01 M/B LA-7811P Schematic | Rev: 1.A

Date: Thursday, June 16, 2011 | Sheet 38 of 63



Sense Pin	Impedance	Codec Signals
SENSE A	20K	PORT1 (PIN 21, 22)
SENSE B	5.1K	PORT-2 (PIN 32, 33)

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: HD Audio Codec ALC663

Size: B | Document Number: *QLA01 M/B LA-7811P Schematic* | Rev: 1.A

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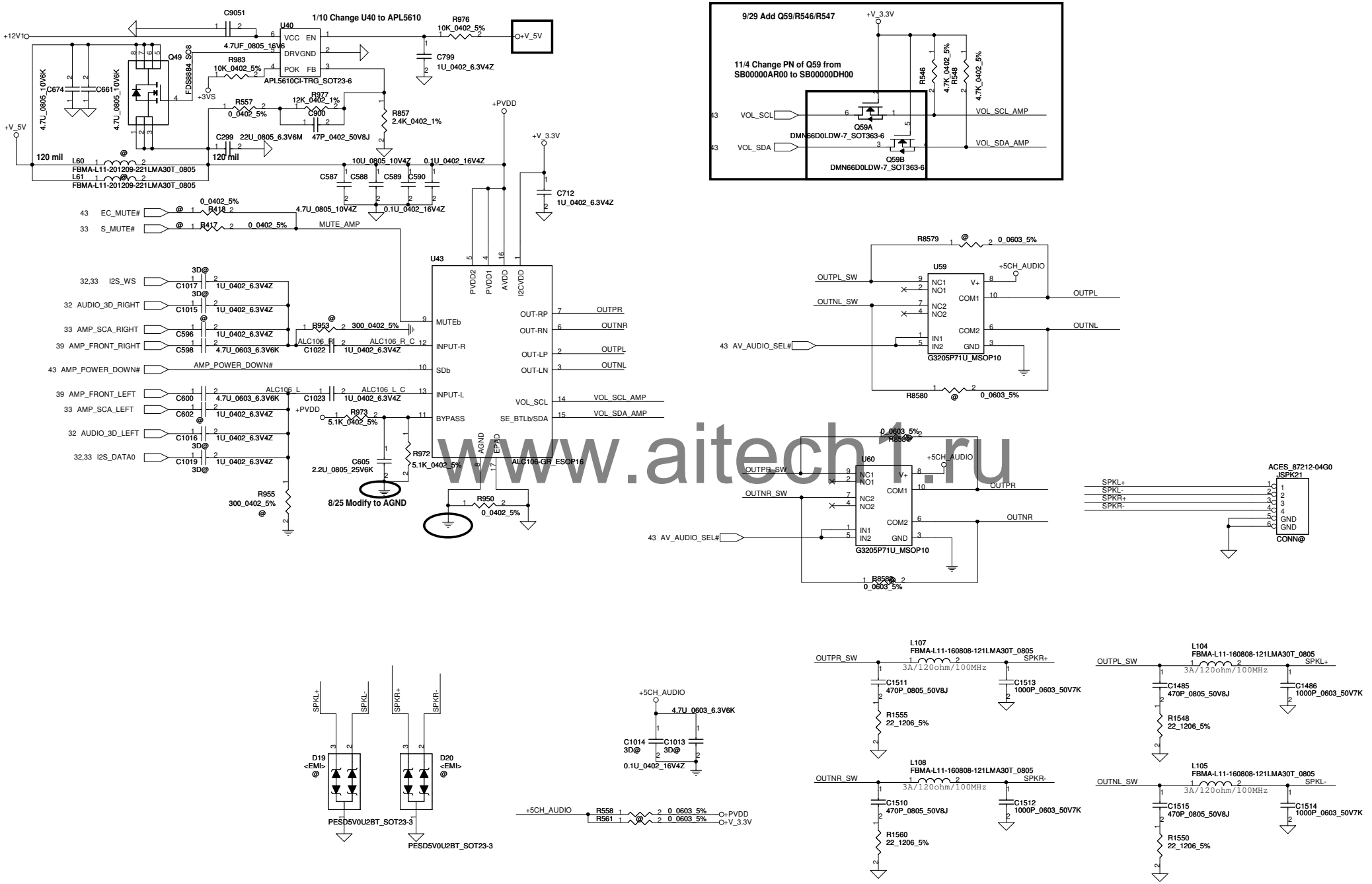

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: AMP

Size: Custom | Document Number: QLA01 M/B LA-7811P Schematic | Rev: 1A

Date: Thursday, June 16, 2011 | Sheet 40 of 63

MIC_L_VREFO

1026 Add Diode for MIC_L_VREFO
12/10 Change symbol of D24/D25 from SC1H751H010 to SCS00002G00

D24 RB751V40_SC76-2
D25 RB751V40_SC76-2

R593 4.7K_0402_5%
R596 4.7K_0402_5%

EXT MIC IN

39 MIC_CEN_R
39 MIC_LFE_L

L30 FBM-11-160808-601-T_0603
L34 FBM-11-160808-601-T_0603

Need
600 Ohm
500 mA

39 MIC_PLUG#
MIC_CEN_R_1
MIC_LFE_L_1

JMIC1 CONN@
SINGATRON 2SJ-B351-S39

C710 330P_0402_50V7K
C711 330P_0402_50V7K
C708 .1U_0402_16V7K ESD request
C647 .1U_0402_16V7K ESD request
Add for EMC suggest

8/13 Change symbol of D30 to SCA00000T00(EMI Suggest)
D30 PESD5V0U2BT_SOT23-3 <EMI>

2/18 Add
R438 0_0603_5% 3D@
R595 0_0603_5% 3D@

2/24 Add
L32 75_0603_1% 3D@
L33 75_0603_1% 3D@

D29 PESD5V0U2BT_SOT23-3 <EMI>
8/13 Change symbol of D29 to SCA00000T00(EMI Suggest)

D28 PESD5V0U2BT_SOT23-3 <EMI>
8/13 Change symbol of D28 to SCA00000T00(EMI Suggest)

HP OUT

33 HP_SCA_RIGHT
33 HP_SCA_LEFT
R824 0_0402_5%
R825 0_0402_5%

39 HP_RIGHT
39 HP_LEFT
R595 2D@ 75_0603_1% INTSPK_CR+
R438 2D@ 75_0603_1% INTSPK_CL+

@R594 20K_0402_5%
@R597 20K_0402_5%

L33 2D@ FBM-11-160808-601-T_0603
L32 2D@ FBM-11-160808-601-T_0603

Need
600 Ohm
500 mA

C646 330P_0402_50V7K
C709 330P_0402_50V7K

33,39,43 HP_PLUG#
PR
PL

JHP1 CONN@
SINGATRON 2SJ-B351-S39

ESD request
C707 .1U_0402_16V7K

8/13 Change symbol of D21 to SCA00000T00(EMI Suggest)
D21 <EMI>
PESD5V0U2BT_SOT23-3

10/22 Change U56 from SA00001ZW00 to SA00004IS00

+PVDD
0.1U_0402_16V4Z
10U_0805_10V6K @ C1005
C806 3D@
3D@ C1002 10U_0805_10V6K

U56 APA2176A
PVDD VDD PGND VSS CVSS GND
CP+ CP- LIN RIN NC
LOUT ROUT /RSD NC /LSD

C1037 3D@ 2.2U_0603_16V6K
C1003 1U_0603_10V6K 3D@
C1004 1U_0603_10V6K 3D@

32 HP_2932_LEFT
32 HP_2932_RIGHT

INTSPK_CL+
INTSPK_CR+
R971 100K_0402_5%
HP_AMP_DOWN#
HP_AMP_DOWN# 43

C1038 2.2U_0603_16V6K 3D@

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: Audio Jack

Size: Custom | Document Number: QLA01 M/B LA-7811P Schematic | Rev: 1.A

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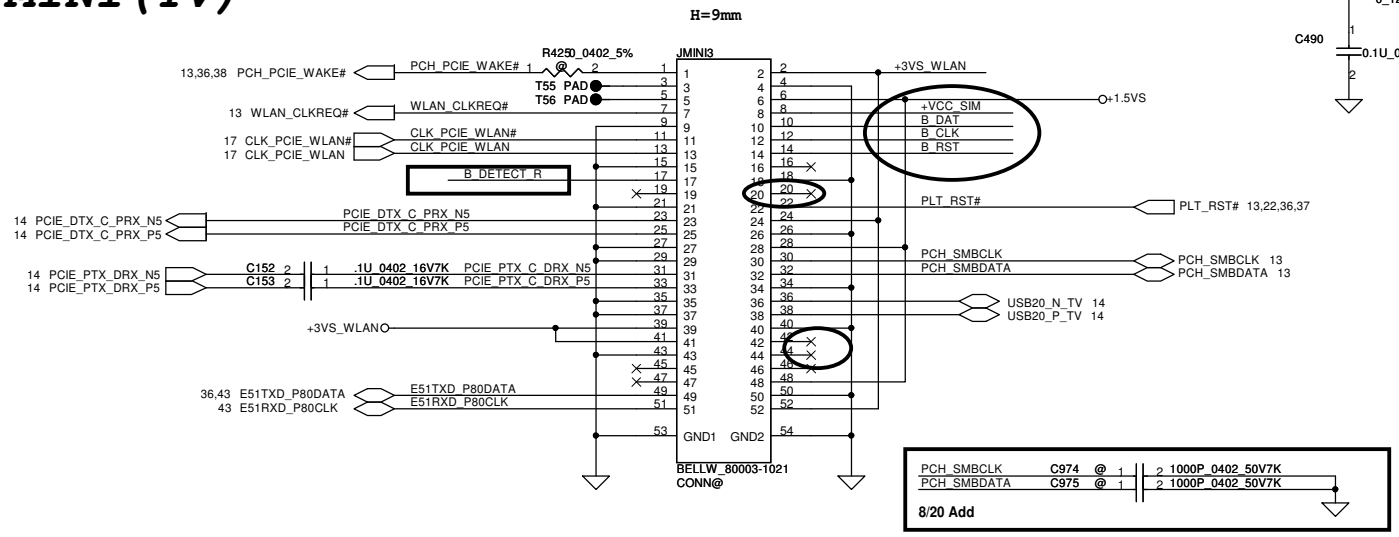
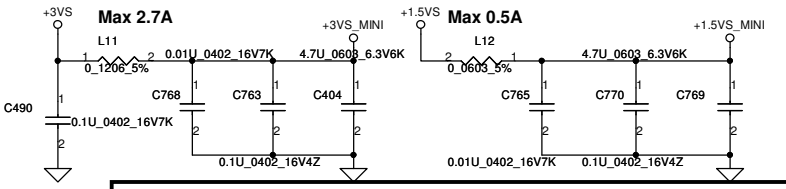
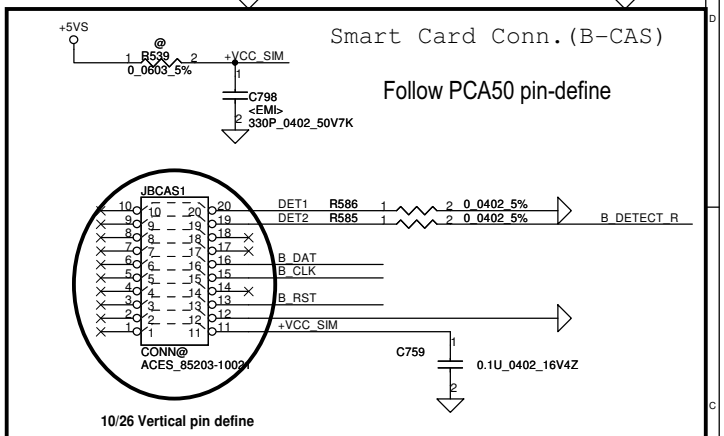
MINI (TV)

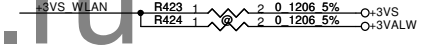
Mini Card Slot 1---TV tuner Currecnt: 3.3 : 2750mA, 1.5: 500mA

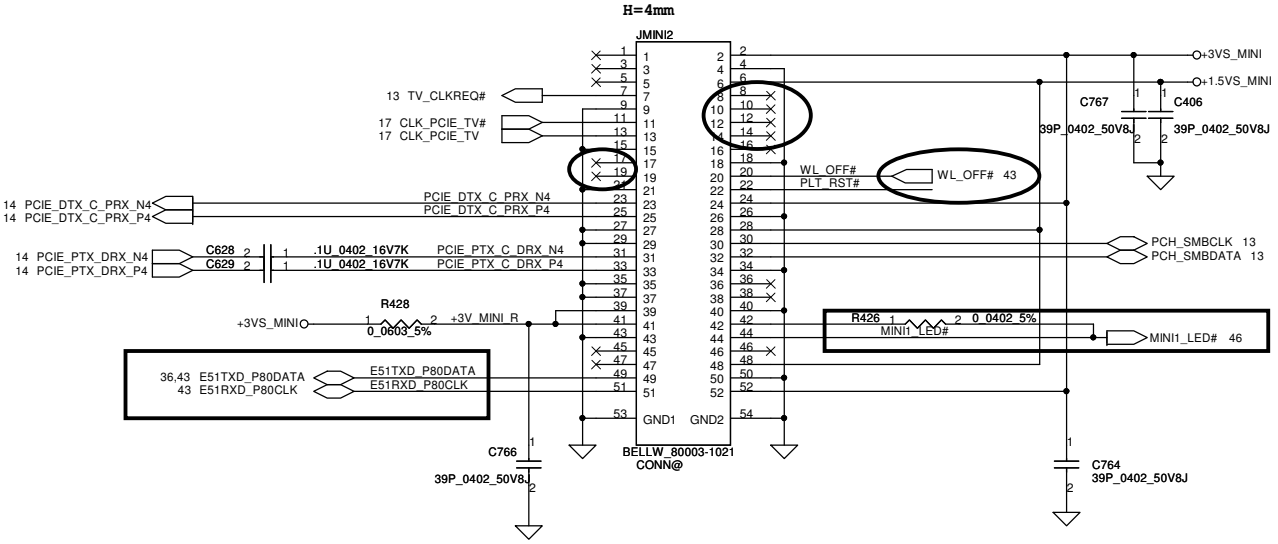


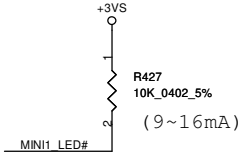


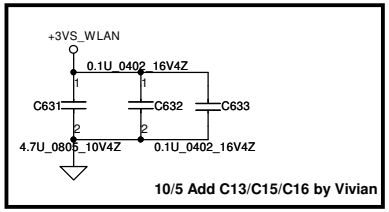


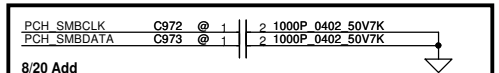
WLAN

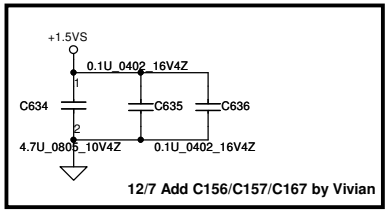












Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: **WLAN&MINI**

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Place closely pin 12

CLK_PCI_LPC — R444 10_0402_5% — C657 18P_0402_50V8J

Place closely pin 13

PCH_PLT_RST# — @ C658 0.1U_0402_16V4Z

C650 1000P_0402_50V7K, C651 0.1U_0402_16V4Z, C652 0.1U_0402_16V4Z, C653 0.1U_0402_16V4Z, C654 0.1U_0402_16V4Z, C655 1000P_0402_50V7K

+3VSB — R552 0_0603_5%

+3VALW — R441 0_0603_5%

+EC_AVCC — C656 0.1U_0402_16V4Z — ECAGND — R443 @ 0_0402_5%

VCC VCC VCC VCC VCC VCC AVCC

U46

KB930QF-A1_LQFP128_14X14

GND GND GND GND GND AGND ECAGND

GATEA20/GPIO00
KBRST#/GPIO01
SERIRQ#
LPC_FRAME#/LFRAME#
LPC_AD3/LAD3
LPC_AD2/LAD2
LPC_AD1/LAD1
LPC_AD0/LAD0
CLK_PCI_EC/PCICLK
PCIRST#/GPIO05
EC_RST#/ECRST#
EC_SCI#/GPIO0E
CLKRUN#/GPIO1D

LPC & MISC

12 EC_GA20 — EC_GA20 1
12 EC_KBRST# — EC_KBRST# 2
12 SERIRQ — SERIRQ 3
13 LPC_FRAME# — LPC_FRAME# 4
13 LPC_AD3 — LPC_AD3 5
13 LPC_AD2 — LPC_AD2 7
13 LPC_AD1 — LPC_AD1 8
13 LPC_AD0 — LPC_AD0 10
17 CLK_PCI_LPC — CLK_PCI_LPC 12
5,13,38 PCH_PLT_RST# — PCH_PLT_RST# 13
+3VSB — R446 47K_0402_5% — ECRST# 37
12 EC_SCI# — EC_SCI# 20
C659 0.1U_0402_16V4Z — 13 CLKRUN# — R925 @ 0_0402_5% — CLKRUN#_R 38

PWM Output

PWM0/GPIO0F — EC_OSD_PWM — EC_OSD_PWM 46
BEEP#/PWM1/GPIO10 — BEEP# — BEEP# 39
FANPWM0/GPIO12 — FAN_CPU_PWM — FAN_CPU_PWM 46
ACOFF/FANPWM1/GPIO13

AD Input

BATT_TEMP/AD0/GPI38 — TV_ON_OFF 32
BATT_OVP/AD1/GPI39 — GFXVR_IMON — GFXVR_IMON 57
ADP_I/AD2/GPI3A — AD_BID
AD3/GPI3B
AD4/GPI42 — IMVP_IMON — IMVP_IMON 57
AD5/GPI43

DA Output

DAC_BRIG/DA0/GPO3C — R762 0_0402_5% — LSADC0 32,33
EN_DFAN1/DA1/GPO3D — R761 0_0402_5% — LSADC1 32,33
IREF/DA2/GPO3E — R449 0_0402_5% — LSADC2 32,33
DA3/GPO3F — R450 0_0402_5% — LSADC3 32,33

PS2 Interface

EC_MUTE#/PSCLK1/GPIO4A — PS2_CLK — PS2_CLK 36
USB_EN#/PSDAT1/GPIO4B — PS2_DATA — PS2_DATA 36
CAP_INT#/PSCLK2/GPIO4C — T86 @
PSDAT2/GPIO4D — T87 @
TP_CLK/PSCLK3/GPIO4E — HP_AMP_DOWN# — EC_3V5V_EN 52
TP_DATA/PSDAT3/GPIO4F — HP_AMP_DOWN# 41

SPI Device I/F

SDICS#/GPXIOA00 — VGATE_R — R453 0_0402_5% — VGATE — VGATE 13,57
WOL_EN/SDICLK/GPXIOA01
ME_EN/SDIMOSI/GPXIOA02 — ME_FLASH 13
LID_SW#/GPXIOD00 — SCALER_ON# 33

SPI Flash ROM

SPIDI/MISO — EC_SI_SPI_SO — EC_SI_SPI_SO 44
SPIDO/MOSI — EC_SO_SPI_SI — EC_SO_SPI_SI 44
SPICLK/GPO58 — SPI_CLK — R454 33_0402_5% — SPI_CLK_R 44
SPICS# — SPI_CS# — SPI_CS# 44

GPIO

GPIO40 — CIR_IN — R455 10K_0402_5% — +3VSB — CIR_IN 46
H_PECI/GPIO41 — H_PECI 5,12
FSTCHG/GPIO50 — GLAN_PCIE_WAKE# — GLAN_PCIE_WAKE# 38
BATT_CHG_LED#/GPIO52 — BT_ON# — BT_ON# 46
CAPS_LED#/GPIO53 — BT_AUTOPAIR — BT_AUTOPAIR 46
BATT_LOW_LED#/GPIO54 — WL_BLUE_LED# — WL_BLUE_LED# 46
PWR_LED#/GPIO55 — PWR_ON_LED# — PWR_ON_LED# 46
SYSON/GPIO56 — SYSON — SYSON 36,47,55
VR_ON/XCLK32K/GPIO57 — VR_ON — VR_ON 57
AC_IN/GPIO59 — PSU_PG# — PSU_PG# 51

SM Bus

EC_SMB_CK1/SCL0/GPIO44
EC_SMB_DA1/SDA0/GPIO45
EC_SMB_CK2/SCL1/GPIO46
EC_SMB_DA2/SDA1/GPIO47

GPIO

EC_RSMRST#/GPXIOA03 — EC_RSMRST# — EC_RSMRST# 13
EC_LID_OUT#/GPXIOA04 — VCCSA_PG — VCCSA_PG 53
EC_ON/GPXIOA05 — EC_ON 48
EC_SWI#/GPXIOA06 — EC_SWI# 13
ICH_PWROK/GPXIOA07 — EC_PWROK — EC_PWROK 13
BKOFF#/GPXIOA08 — BKOFF# — BKOFF# 34
RF_OFF#/GPXIOA09 — EC_ID — WL_OFF# 42
GPXIOA11 — POWER_KEY — POWER_KEY 33

GPO

GPI

PM_SLP_S4#/GPXIOD01 — ENBKL — PM_SLP_S4# 13
ENBKL/GPXIOD02 — R461 0_0402_5% — S_BKOFF 32,33,34
EAPD/GPXIOD03 — EAPD_CODEC 39
EC_THERM#/GPXIOD04 — HDMI_CABLE_DET — HDMI_CABLE_DET 36
SUSP#/GPXIOD05 — SUSP# 47,53,54,56,59
PBTN_OUT#/GPXIOD06 — PBTN_OUT# 13
EC_PME#/GPXIOD07 — 35V_PG — 35V_PG 52

V18R — C663 4.7U_0603_6.3V6K

Int. K/B Matrix

KSI0/GPIO30
KSI1/GPIO31
KSI2/GPIO32
KSI3/GPIO33
KSI4/GPIO34
KSI5/GPIO35
KSI6/GPIO36
KSI7/GPIO37
KSO0/GPIO20
KSO1/GPIO21
KSO2/GPIO22
KSO3/GPIO23
KSO4/GPIO24
KSO5/GPIO25
KSO6/GPIO26
KSO7/GPIO27
KSO8/GPIO28
KSO9/GPIO29
KSO10/GPIO2A
KSO11/GPIO2B
KSO12/GPIO2C
KSO13/GPIO2D
KSO14/GPIO2E
KSO15/GPIO2F
KSO16/GPIO48
KSO17/GPIO49

39 CODEC_ON — KSO3 42
46 EC_OSD_RST# — EC_OSD_RST# 43
46 SOURCE_LED — SOURCE_LED 44
34 EC_CAM_OFF — EC_CAM_OFF 45
40 AV_AUDIO_SEL# — AV_AUDIO_SEL# 46
51,55 S3_1.5VEN — S3_1.5VEN 47
34 EC_ENVDD — EC_ENVDD 48
32 3D_PWREN — 3D_PWREN 49
18 PCH_ENABLE — PCH_ENABLE 50
J8 @ 10K 0603 5% 52
32,33 PANEL_STATE_OFF — UART_RX_R 54
12 EC_REVPWROK — H_PROCHOT# EC 82
EC_REVPWROK

40 VOL_SCL — VOL_SCL 77
40 VOL_SDA — VOL_SDA 78
13 EC_SMB_CK2_M — EC_SMB_CK2_M 79
13 EC_SMB_DA2_M — EC_SMB_DA2_M 80

13 PM_SLP_S3# — PM_SLP_S3# 6
13 PM_SLP_S5# — PM_SLP_S5# 14
13,36 EC_SMI# — EC_SMI# 15
46 EC_ESB_INT — EC_ESB_INT 16
46 EC_OSD_CK — 17
46 EC_OSD_DA — 18
13 SUS_PWR_ACK — SUS_PWR_ACK 19
34 INVT_PWM — INVT_PWM 25
46 FAN_CPU_SPEED — FAN_CPU_SPEED 28
E51TXD_P80DATA 29
36,42 E51TXD_P80DATA — E51TXD_P80DATA 30
42 E51RXD_P80CLK — E51RXD_P80CLK 31
48 ON/OFF — ON/OFF 32
46 CEN_PWR_LED — CEN_PWR_LED 34
13 SUSWARN# — SUSWARN# 36

PM_SLP_S3#/GPIO04
PM_SLP_S5#/GPIO07
EC_SMI#/GPIO08
GPIO0A
GPIO0B
GPIO0C
SUS_PWR_DN_ACK/GPIO0D
INVT_PWM/PWM2/GPIO11
FAN_SPEED1/FANFB0/GPIO14
FANFB1/GPIO15
EC_TX/GPIO16
EC_RX/GPIO17
ON_OFF/GPIO18
SUSP_LED#/GPIO19
NUM_LED#/GPIO1A

C662 15P_0402_50V8J — CRY2 122
32.768KHZ_12.5PF_Q13MC14610002 — XCLK1 123
XCLK0
NC OSC NC OSC — Y6
@ R463 20M_0402_5%
C664 15P_0402_50V8J — CRY1
R467 0_0402_5% @
13 PCH_SUSCLK

JP1

KSO2 1
KSO3 2
KSI6 3
KSI4 4
KSI6 5
KSI7 6
E51TXD_P80DATA 7
8
9 G1
10 G2

MOLEX 514410893 8P H1.1 FPC S H-CONN @

EC DEBUG port

Reserve R460 for EC debug.

R460 — E51TXD_P80DATA — 100K_0603_5%

10/25 Add R968

+3VSB — 4.7K_0402_5% — R968 — KSI7

8/15 Add

15,32,33 UART_TX — R474 0_0402_5% — UART_TX_R
15,32,33 UART_RX — R485 0_0402_5% — UART_RX_R

8/19 Add R884(Vendor suggest)

1K_0402_1% — R884 — PANEL_STATE_OFF

1000P_0402_50V7K — @ C982 — EC_SMB_CK2
1000P_0402_50V7K — @ C983 — EC_SMB_DA2

8/20 Add

100P_0402_50V8J — C876 — ON/OFF

+3VSB — @ R465 10K_0402_5% — U39 @ SN74AHCT1G125GW_SOT353-5 — EC_RSMRST#
@ C665 0.1U_0402_10V6K
R471 0_0402_5% @

+V_3.3V — R550 4.7K_0402_5% — R551 4.7K_0402_5%

EC_SMB_CK2_M — Q61A DMN66D0LDW-7_SOT363-6 — EC_SMB_CK2 — EC_SMB_CK2 21
EC_SMB_DA2_M — Q61B DMN66D0LDW-7_SOT363-6 — EC_SMB_DA2 — EC_SMB_DA2 21

VR_HOT# — R447 0_0402_5% @ — H_PROCHOT# 5
H_PROCHOT#_EC — Q42 2N7002H_SOT23 — C860 47P_0402_50V8J

TV_ON_OFF — C675 0.1U_0402_16V4Z

+3VSB — Ra R442 100K_0402_5% AV@ — AD_BID — Rb R445 0_0603_5% NON_AV@

LSADC0 R492 100K_0402_5%
LSADC1 R493 100K_0402_5%
LSADC2 R494 100K_0402_5%
LSADC3 R495 100K_0402_5%

10/5 Add R492~495(EC request)

9/29 Change net name from +V_5V to +5VSB

+5VSB
PS2_CLK — 4.7K_0402_5% — @ R927
PS2_DATA — 4.7K_0402_5% — @ R928

PCH_PLT_RST# — R456 100K_0402_5%

R458 2D@ 100K_0402_5% — +3VSB
R459 3D@ 100K_0402_5%

+3VSB

EC_OSD_RST#	2.2K_0402_5%	R947
BT_RESET	4.7K_0402_5%	R941
AV_AUDIO_SEL#	4.7K_0402_5%	3D@ R936
HDMI_CABLE_DET	4.7K_0402_5%	R887
EC_OSD_CK	4.7K_0402_5%	R854
EC_OSD_DA	4.7K_0402_5%	R853
PANEL_STATE_OFF	4.7K_0402_5%	@ R497
AMP_POWER_DOWN#	4.7K_0402_5%	R496
EC_ESB_INT	2.2K_0402_5%	R771
GLAN_PCIE_WAKE#	100K_0402_5%	R462
ON/OFF	4.7K_0402_5%	R464
POWER_KEY	4.7K_0402_5%	R713
PWR_ON_LED#	8.2K_0402_5%	R466
VOL_SCL	4.7K_0402_5%	R468
VOL_SDA	4.7K_0402_5%	R469
WL_BLUE_LED#	8.2K_0402_5%	R470
EC_MUTE#	4.7K_0402_5%	R472
TV_ON_OFF	4.7K_0402_5%	R481

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: EC KB930/KB conn

Size: Custom | Document Number: QLA01 M/B LA-7811P Schematic | Rev: A

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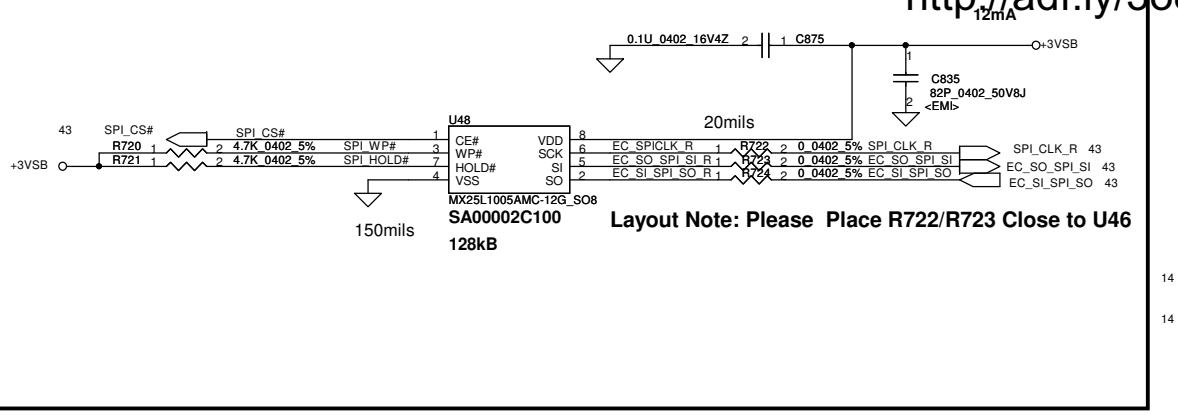
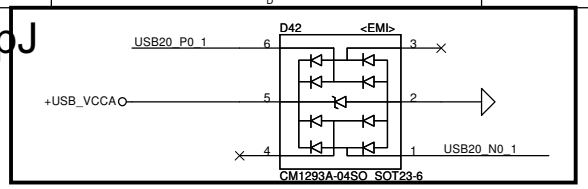
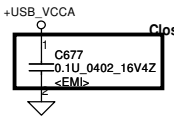
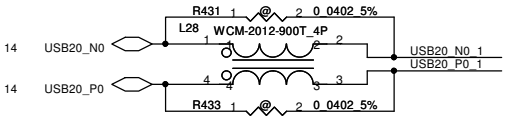
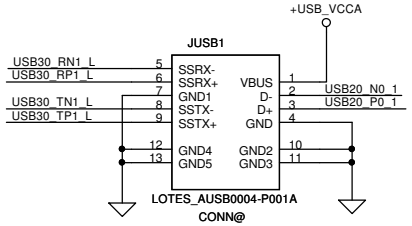




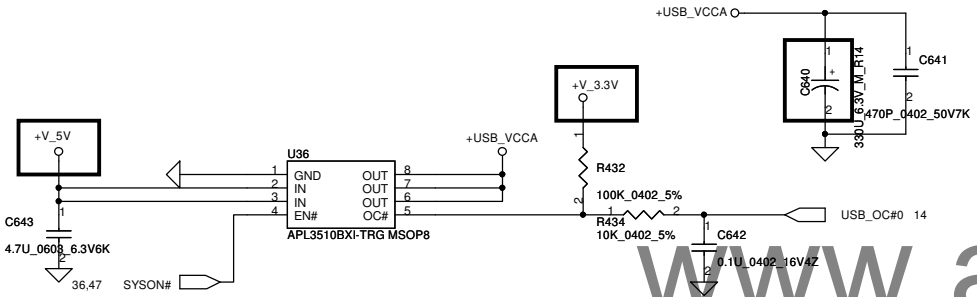
10/25 Change symbol and footprint of D42 from SC300000100 to SC300000O00(ESD request)

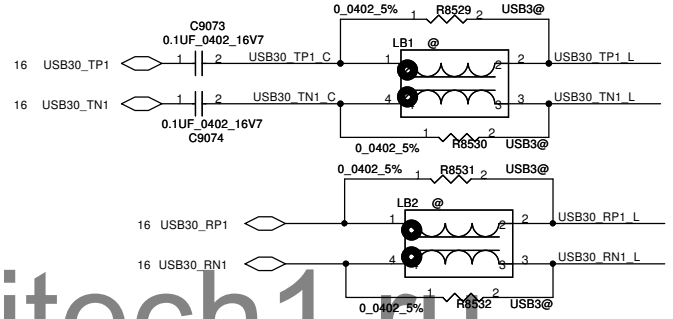


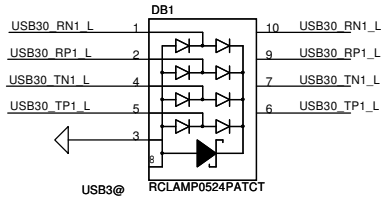




11/2 Change PN of C640 from SF000002Y00 to SF000001G00

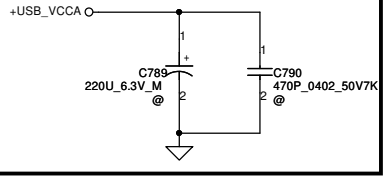




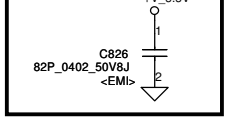


Part Number = SC300000T10

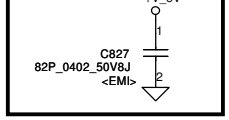
10/3 Add C789/C790(Place close to JP10)

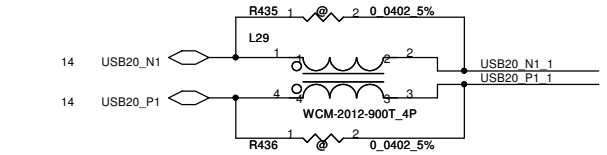


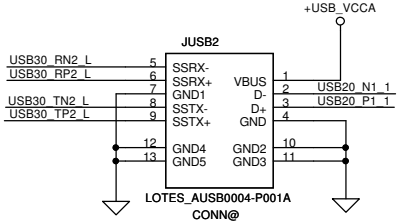
10/22 Add(EMI Request)



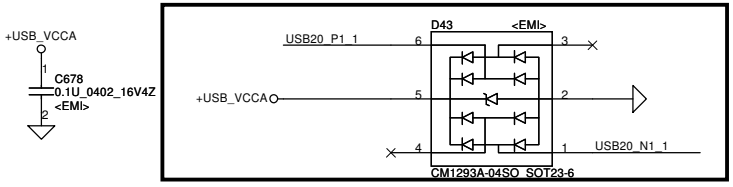
10/22 Add(EMI Request)



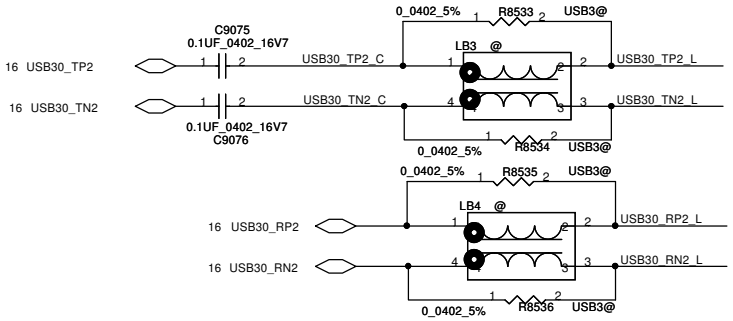


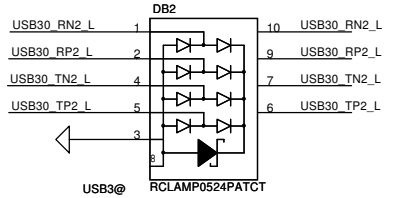


8/13 Add D43/C678(EMI Suggest)



10/25 Change symbol and footprint of D43 from SC300000100 to SC300000O00(ESD request)





Part Number = SC300000T10

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: USB / BIOS ROM

Size: Custom | Document Number: QLA01 M/B LA-7811P Schematic | Rev: 1.A

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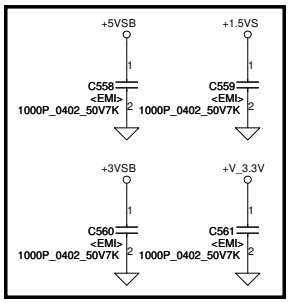
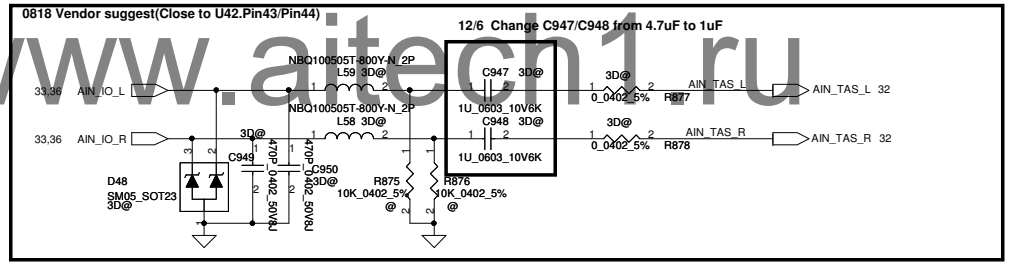
10/27 Add C558~C561(EMI request)



0818 Vendor suggest(Close to U42.Pin43/Pin44)

12/6 Change C947/C948 from 4.7uF to 1uF



De-Emphasis Control		
DEMT1 (pin 17)	DEMT0 (pin 16)	AUDIO INTERFACE
LOW	LOW	OFF *
LOW	HIGH	48 kHz
HIGH	LOW	44.1 kHz
HIGH	HIGH	32 kHz

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: 5CH AUDIO_PCM1606

Size: Custom | Document Number: QLA01 M/B LA-7811P Schematic | Rev: A

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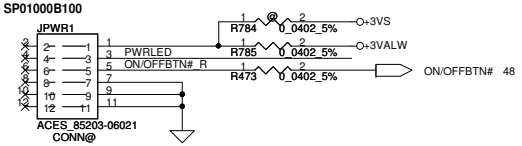
Power switch board

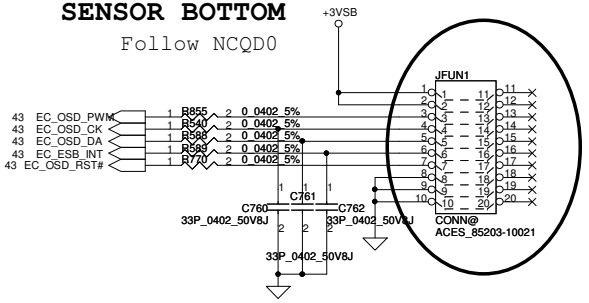
12/6 Change symbol of JPWR1 from SP02000U100 to SP01000B100



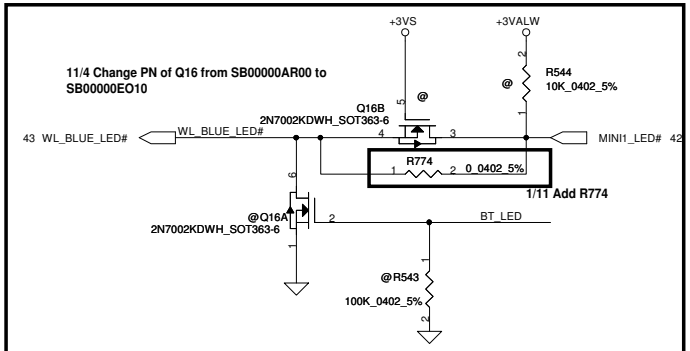
SENSOR BOTTOM

Follow NCQD0

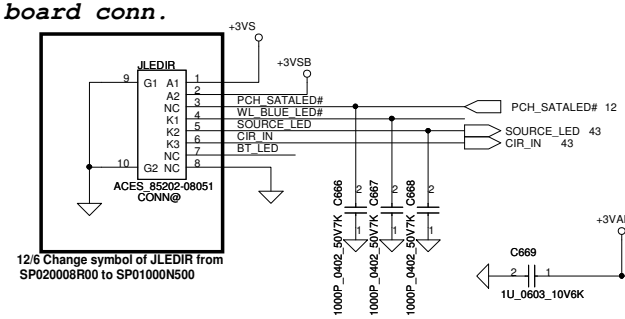
12/6 Change symbol of JFUN1 from SP02000AN00 to SP01000HE00



11/4 Change PN of Q16 from SB00000AR00 to SB00000EO10

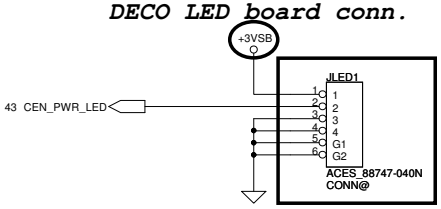


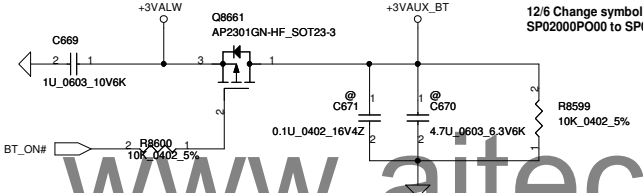
LED board conn.



12/6 Change symbol of JLEDIR from SP020008R00 to SP01000N500

DECO LED board conn.

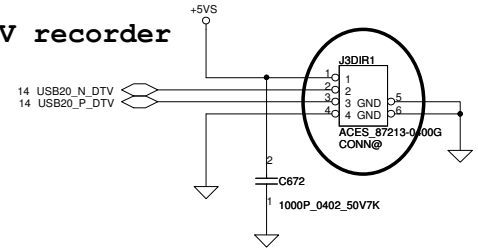




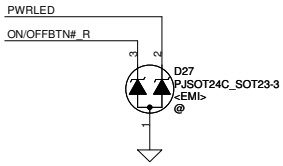
12/6 Change symbol of JLED1 from SP02000PO00 to SP010028400(3pin to 4 pin)

10/3 Change symbol of J3DIR1 from SP020008V00 to SP02000GC00(直立式 to R/A)

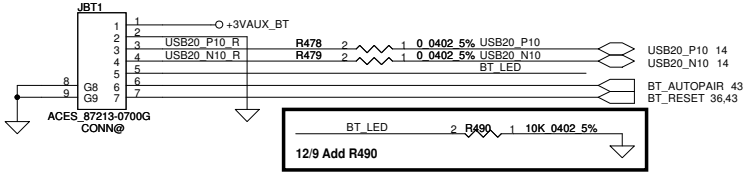
DTV recorder



8/13 Change symbol of D27 to SCA00000E00(EMI Suggest)

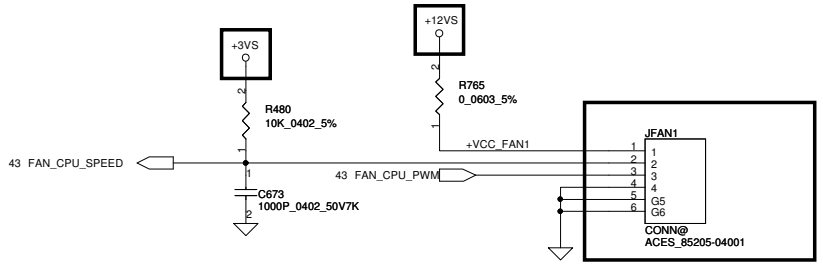


10/26 Change symbol and footprint of JBT1 from SP02000FR00 to SP02000F000



BT Connector

Fan Control circuit



11/29 Change symbol and footprint of JFAN1 from SP02000U900 to SP020008X00

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: WL/BT ON/OFF, PWR S/W, OSD

Size	Document Number	Rev
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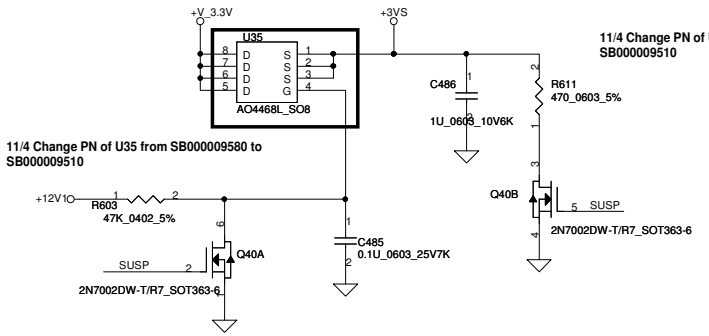
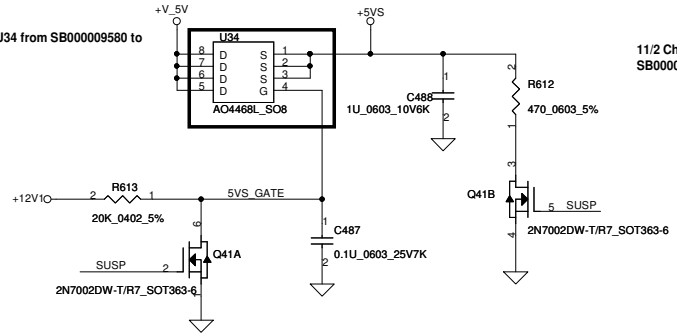
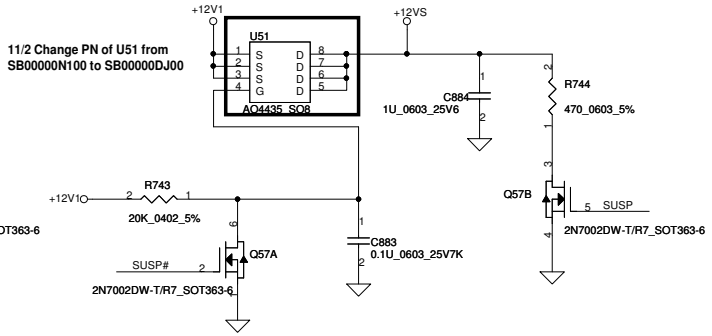
+V_3.3V TO +3VS



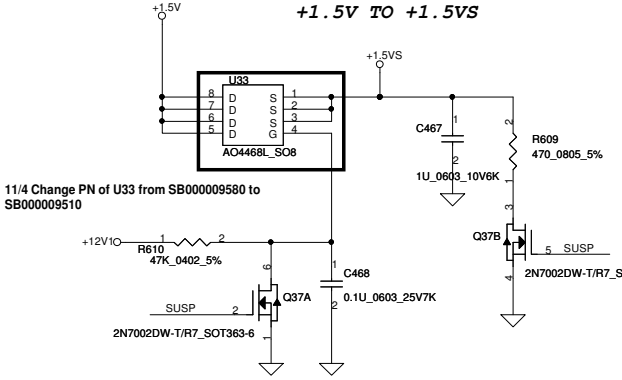
+V_5V TO +5VS

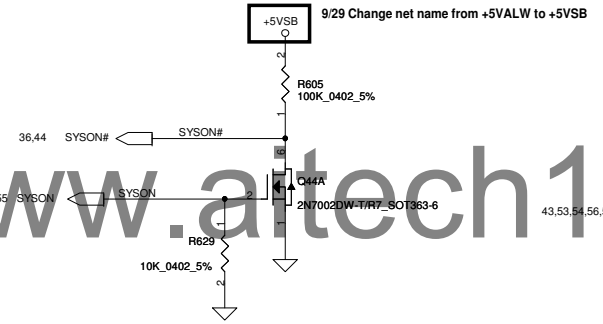


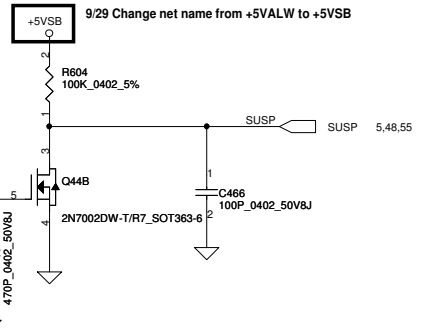
+12V1 TO +12VS



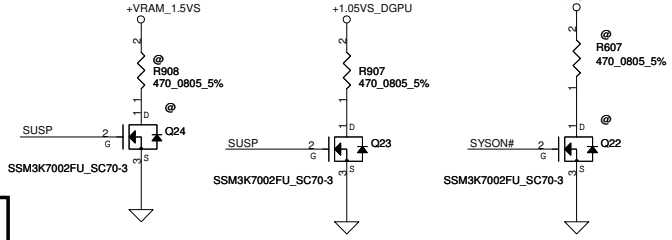
+1.5V TO +1.5VS

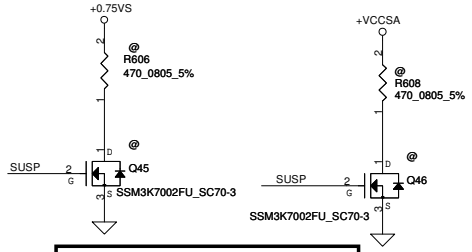


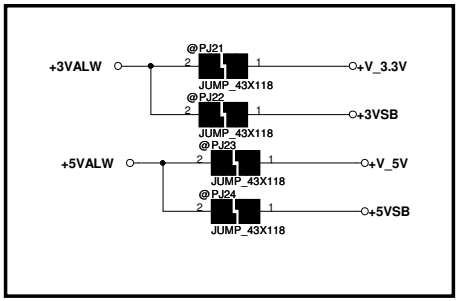




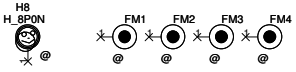
Discharge circuit



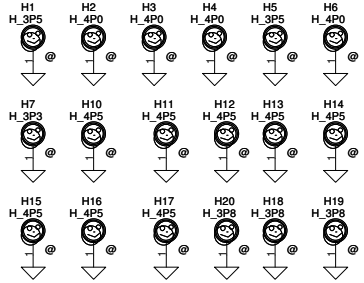




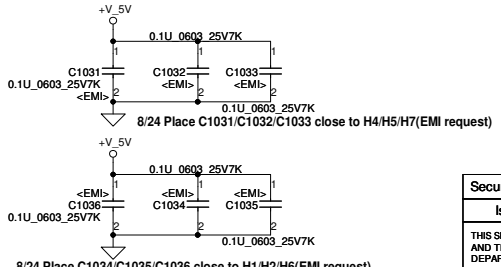
NON-PDH



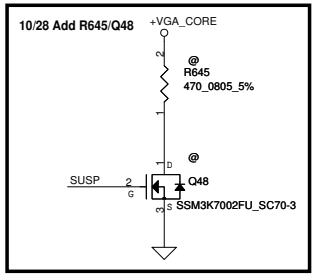
Screw



8/24 Add C1031~C1036



10/28 Add R645/Q48



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: DC Interface/Screw

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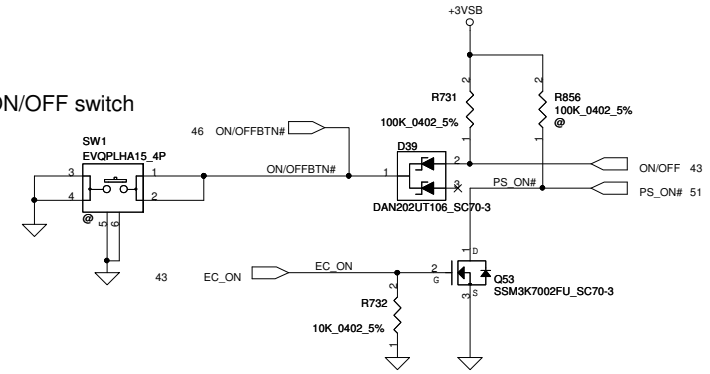
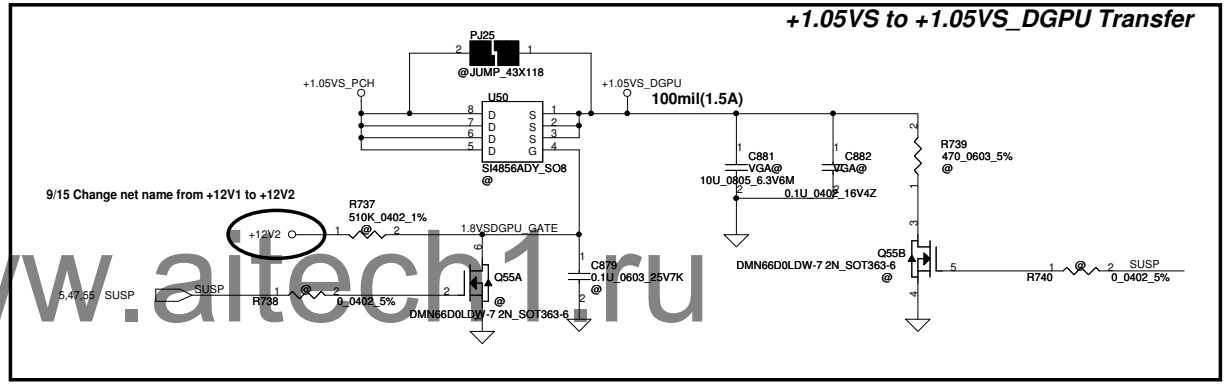
http://adf.ly/3o8pJ

Power Button

ON/OFF switch



+1.05VS to +1.05VS_DGPU Transfer



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/07/20	Deciphered Date 2011/07/20	Title: Power OK/PBN
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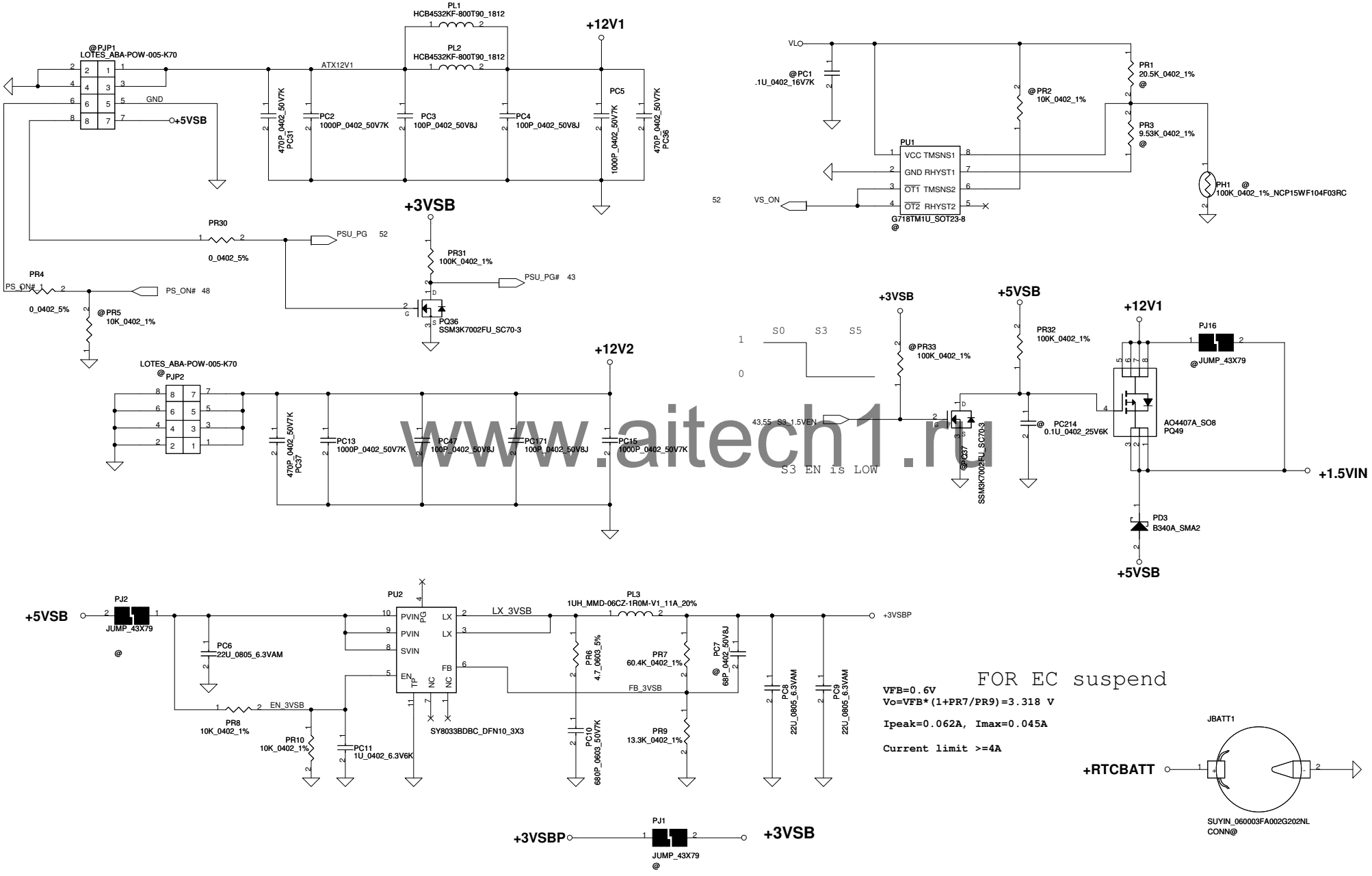
			Date: Thursday, June 16, 2011; Sheet 48 of 63

PH1 under CPU botten side :

CPU thermal protection at 92 degree C
Recovery at 57 degree C



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title

Size	Document Number	Rev
Custom		0.1

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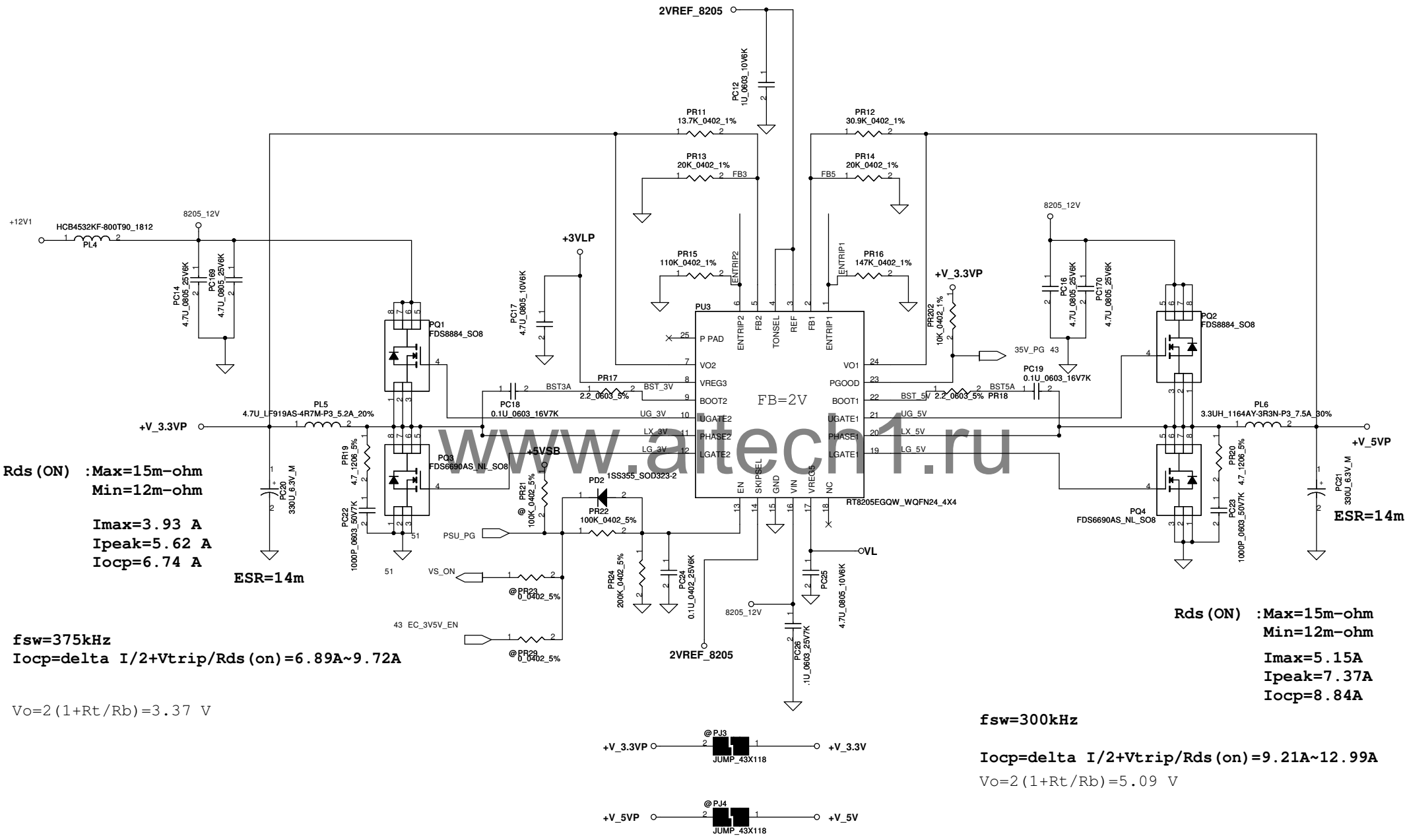


Rds(ON) :Max=15m-ohm
Min=12m-ohm

Imax=3.93 A
Ipeak=5.62 A
Iocp=6.74 A

ESR=14m

fsw=375kHz
Iocp=delta I/2+Vtrip/Rds(on)=6.89A~9.72A

Vo=2(1+Rt/Rb)=3.37 V

Rds(ON) :Max=15m-ohm
Min=12m-ohm

Imax=5.15A
Ipeak=7.37A
Iocp=8.84A

ESR=14m

fsw=300kHz

Iocp=delta I/2+Vtrip/Rds(on)=9.21A~12.99A

Vo=2(1+Rt/Rb)=5.09 V

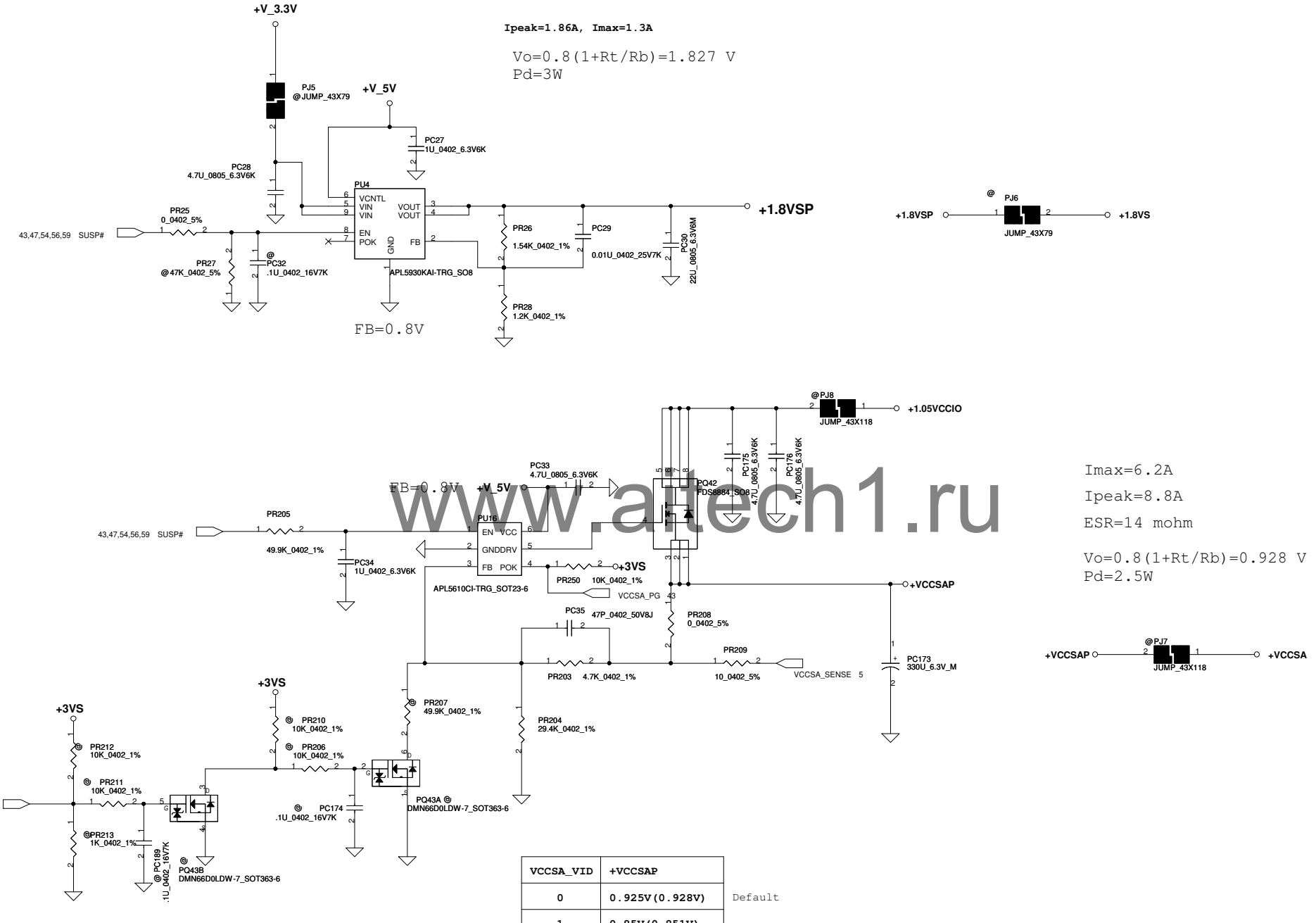
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: **+V_5VP/ +V_3VP**

Size	Document Number	Rev
Custom		0.1

Date: Thursday, June 16, 2011 | Sheet 52 of 63



VCCSA_VID	+VCCSAP	
0	0.925V(0.928V)	Default
1	0.85V(0.851V)	

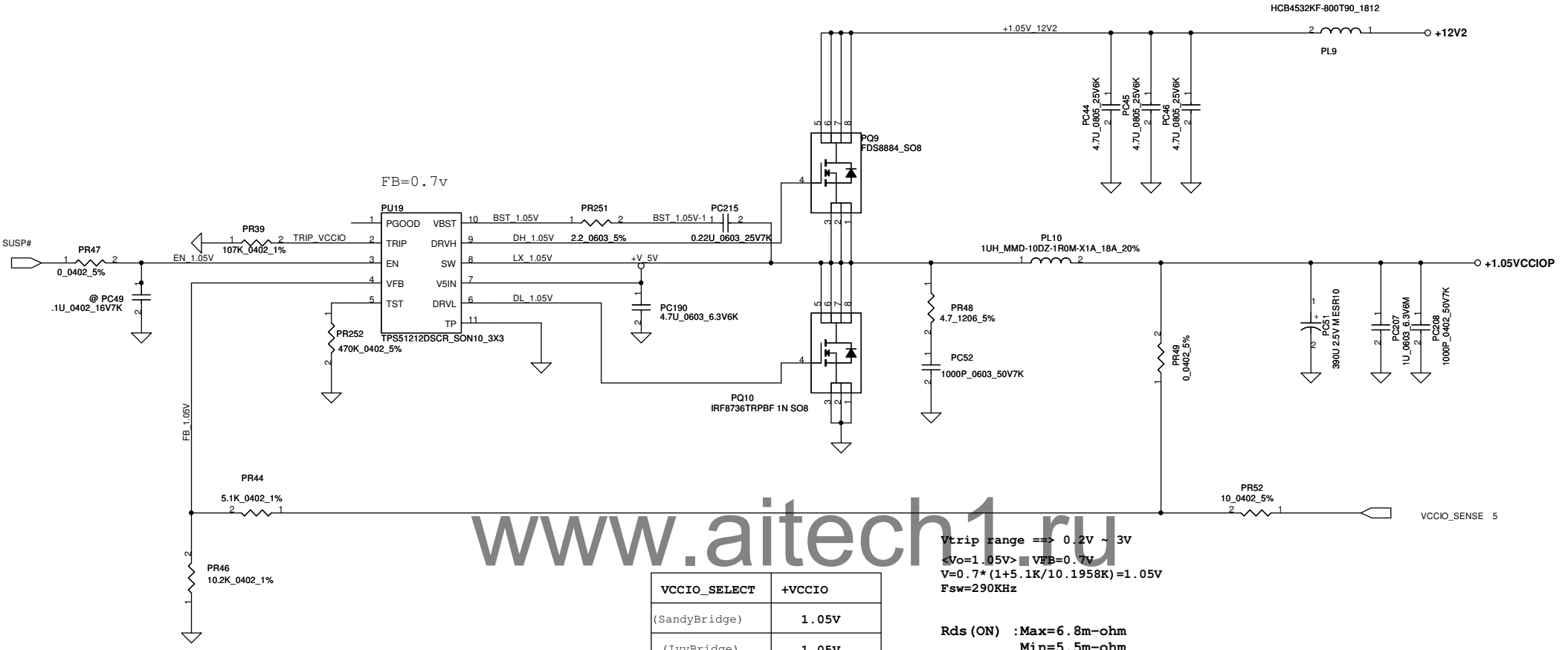
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: +VCCSA/+1.8VSP

Size	Document Number	Rev
Custom		0.1

Date: Thursday, June 16, 2011 | Sheet 53 of 63



VCCIO_SELECT	+VCCIO
(SandyBridge)	1.05V
(IvyBridge)	1.05V

Vtrip range ==> 0.2V ~ 3V
<Vo=1.05V> VFB=0.7V
V=0.7*(1+5.1K/10.1958K)=1.05V
Fsw=290KHz

Rds(ON) :Max=6.8m-ohm
Min=5.5m-ohm

Imax=11.17 A
Ipeak=15.96 A
Iocp= 19.15A

1.05V, Iocp=delta I/2+Vtrip/Rds(on)=19.35A~28.4A

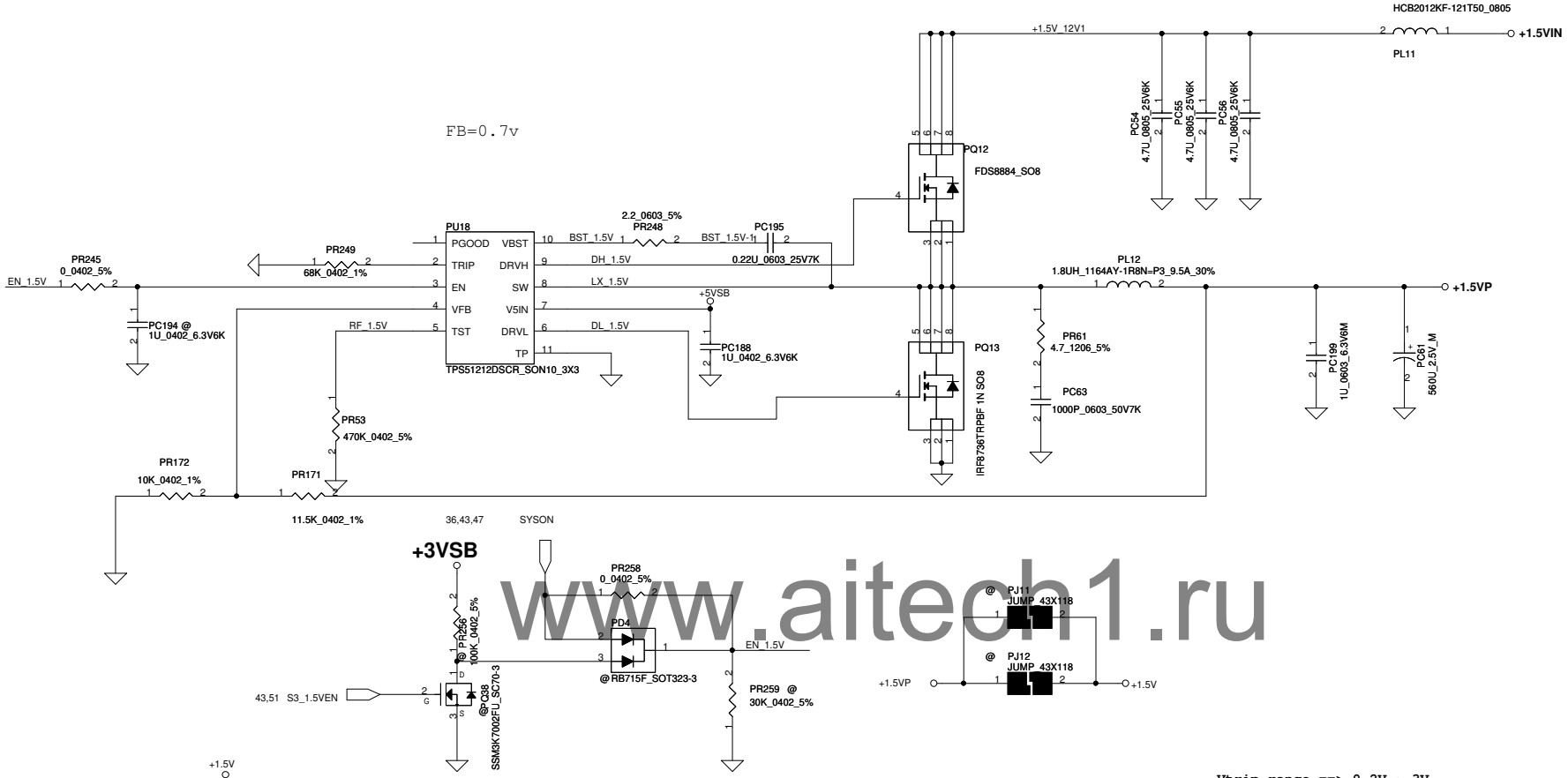
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: +1.05VSP

Size: Custom | Document Number | Rev: 0.1

Date: Thursday, June 16, 2011 | Sheet 54 of 63



Vtrip range ==> 0.2V ~ 3V

Ipeak=10.24A Imax=7.168A
Iocp >=1.2*Ipeak=12.3A

<Vo=1.5V> VFB=0.7V
Vo=VFB*(1+Rtop/Rdown)=1.505V
Fsw=290 KHz
Cout ESR=15m ohm Rdson(max)=6.8m ohm, Rdson(typ)=5.5 mohm

Delta I=((19-1.5)*(1.5/19))/(1.8u*290 K)=?? A
=>1/2DeltaI=??A
Vtrip=Itrip*Rtrip, Iocp=Vtrip/(8*Rds(on))
Iocpmax=((95.3K*11uA)/(8*0.0055))+1.3233A=??A
 Iocpmin=((95.3K*9uA)/(8*0.0068)+1.3233A=??A
Iocp=12.5A~18.2A

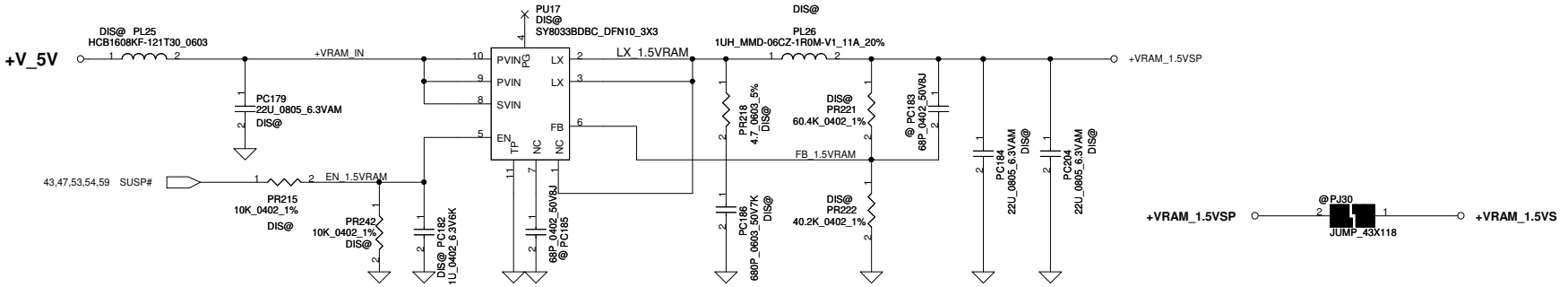
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: 1.5VP/+1.2VALWP/+0.75VS

Size: Custom | Document Number | Rev: 0.1

Date: Thursday, June 16, 2011 | Sheet 55 of 63



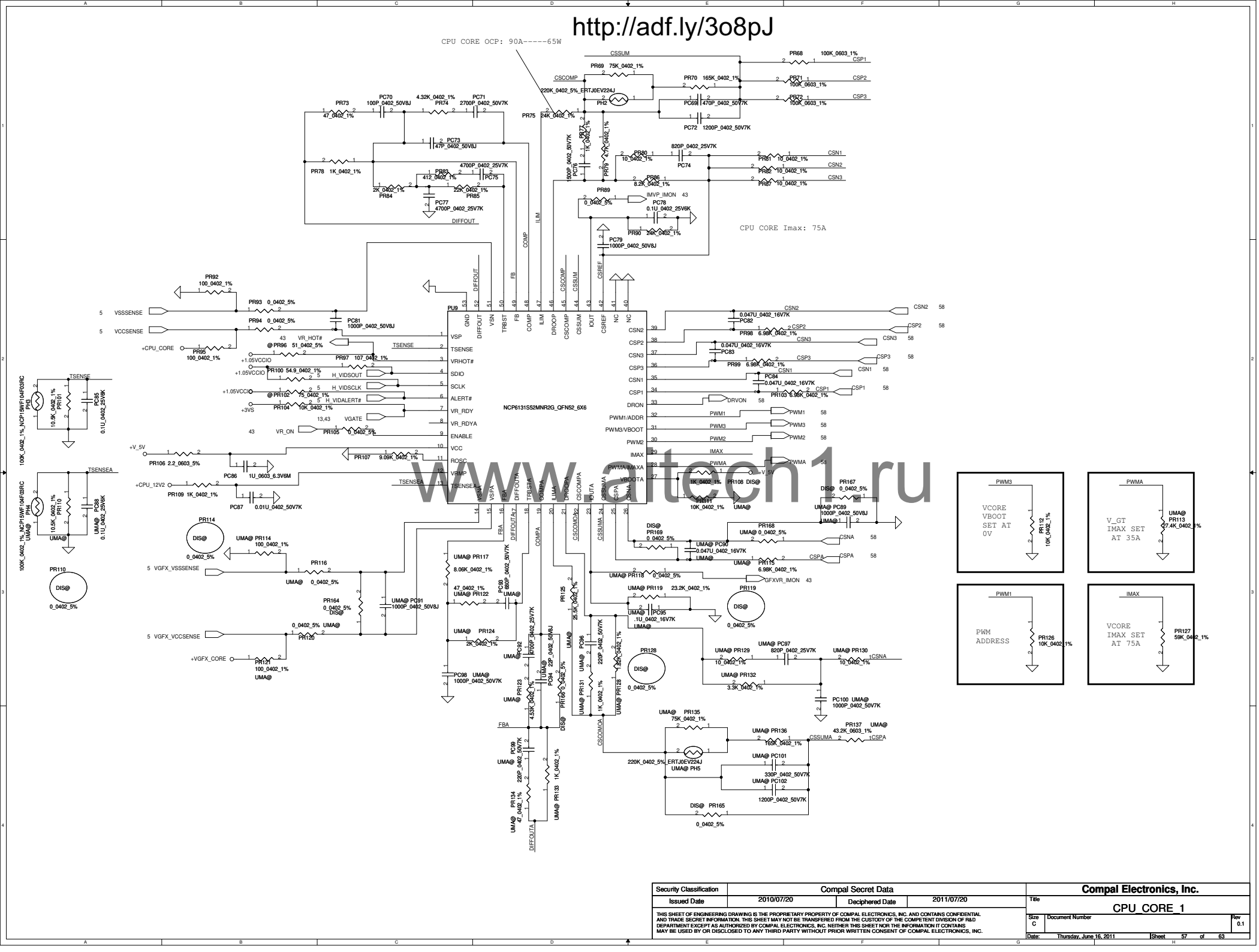
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: VCCPP/1.8VP

Size: Custom | Document Number: QLA01 M/B LA-7811P Schematic | Rev: 0p

Date: Thursday, June 16, 2011 | Sheet 56 of 63



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: CPU_CORE_1

Size	Document Number	Rev
C		0.1

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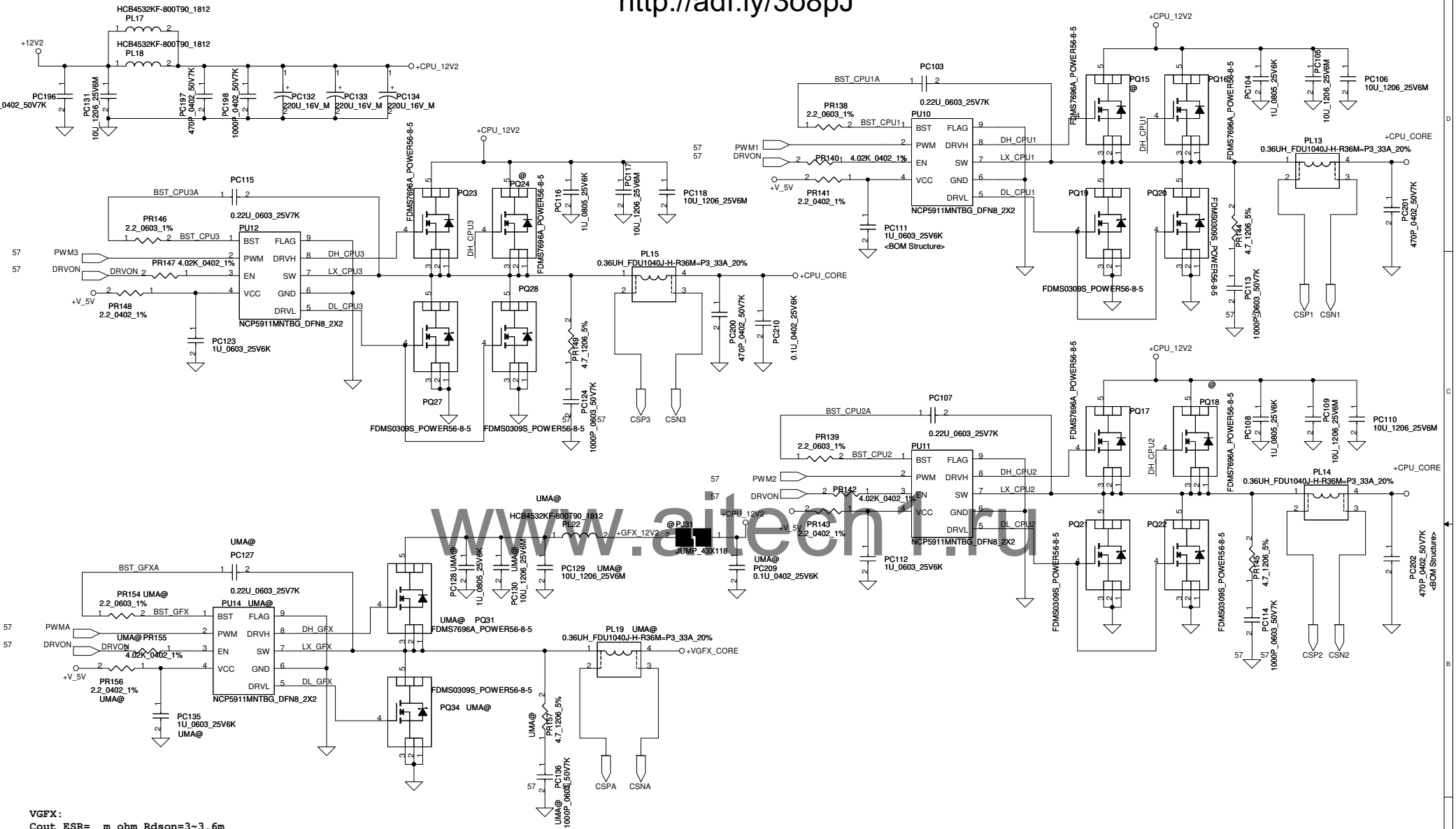

VGFX:
Cout ESR= m ohm Rdson=3~3.6m
Ipeak=35 A, Imax=25 A
Delta I=7A

OCP= 40 A

CPU_CORE:
Cout=22U*18+ 390u 10m*4+560u 10m*3 +330u 9m*3 +560u 15m*2
Rdson=3~3.6m
Ipeak= A, Imax=85 A
F=338k hz
Delta I=

OCP= 135 A

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

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Title: CPU_CORE_2

Size	Document Number	Rev
Custom		0.1

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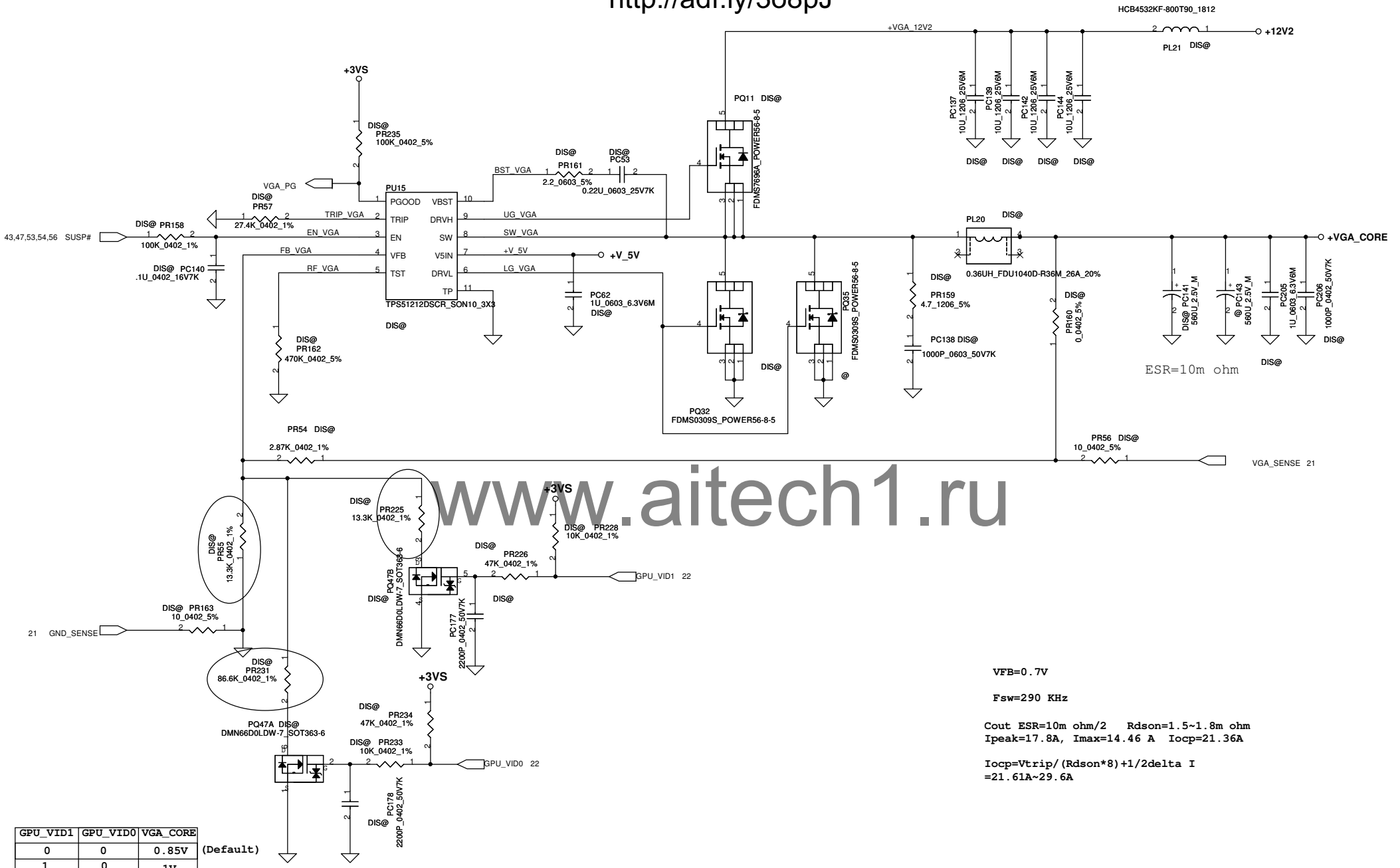

GPU_VID1	GPU_VID0	VGA_CORE
0	0	0.85V (Default)
1	0	1V
1	1	1.025V

VFB=0.7V

Fsw=290 KHz

Cout ESR=10m ohm/2 Rdson=1.5~1.8m ohm
Ipeak=17.8A, Imax=14.46 A Iocp=21.36A

Iocp=Vtrip/(Rdson*8)+1/2delta I
=21.61A~29.6A

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: VGA_CORE

Size: Custom | Document Number | Rev: 0.1

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